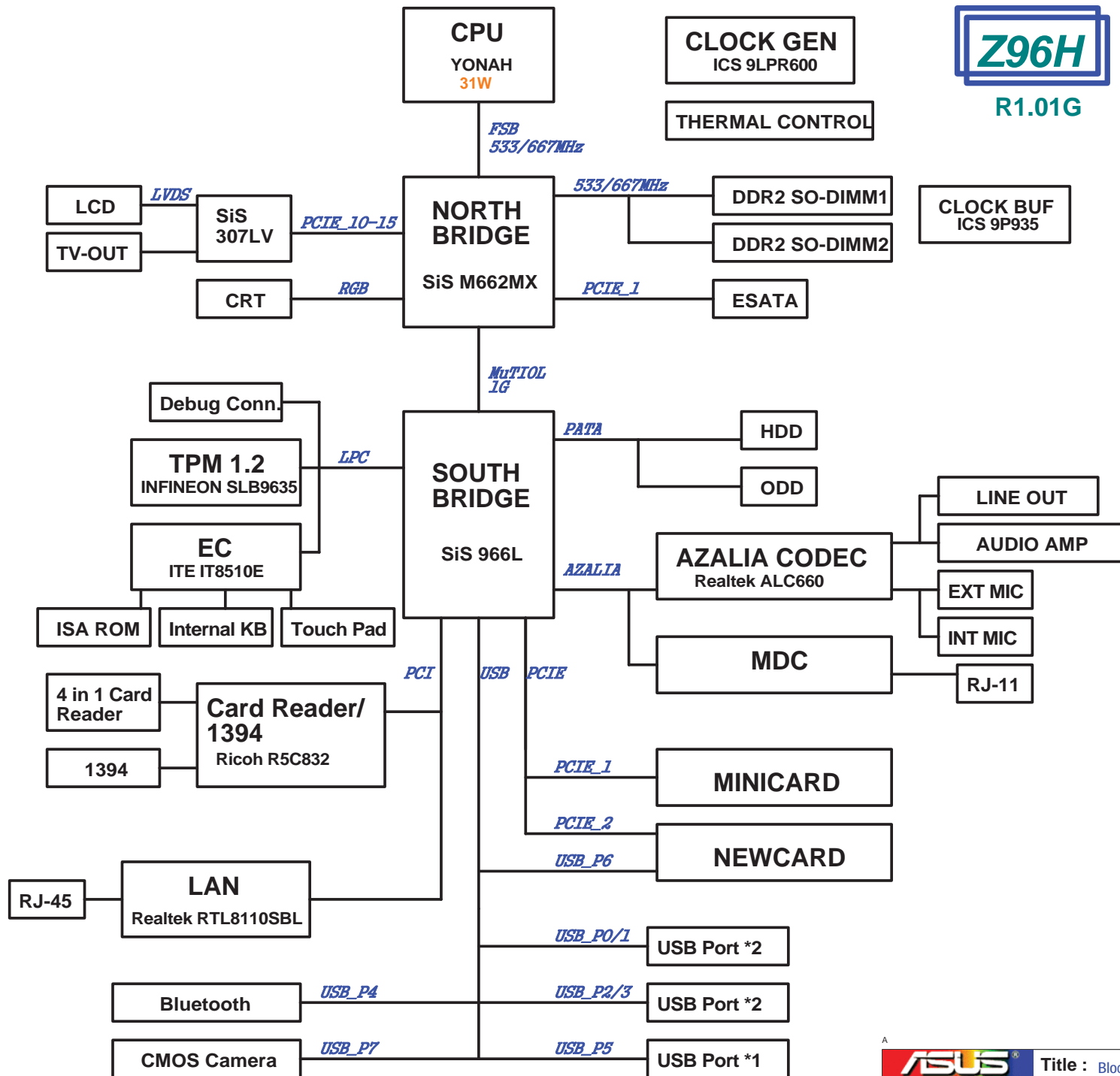


01\_Block Diagram  
 02\_System Setting  
 03\_Power Sequence  
 04\_History  
 07\_CLOCK GEN-ICS9LPR600  
 08\_CLOCK BUFFER-ICS9P935  
 09\_CPU-YONAH(HOST)  
 10\_CPU-YONAH(PWR)  
 11\_NB-M662MX(HOST)  
 12\_NB-M662MX(MuTIO&VGA)  
 13\_NB-M662MX(PCIE)  
 14\_NB-M662MX(DDR2)  
 15\_NB-M662MX(PWR)  
 16\_NB-M662MX(GND)  
 17\_SB-966L(PCI-IDE-MuTIO)  
 18\_SB-966L(PCIE-AZALIA-MII)  
 19\_SB-966L(USB-SATA)  
 20\_SB-966L(PWR-GND)  
 21\_SB-966L(OTHER)  
 22\_DDR2 SO-DIMM0  
 23\_DDR2 SO-DIMM1  
 24\_DDR2 TERMINATION  
 25\_SiS 307LV(OpenLDI&TV)  
 26\_CRT  
 27\_LVDS & INVERTER CONNECTOR  
 28\_TV OUT CONN  
 29\_HDD & ODD  
 30\_MINICARD  
 31\_NEWCARD  
 32\_ESATA  
 33\_CARD1394-R5C832(1)  
 34\_CARD1394-R5C832(2)  
 35\_4 in 1 CARD READER  
 36\_LAN-RTL8110SBL  
 37\_MDC&RJ45&RJ11  
 38\_CODEC-ALC660  
 39\_AUDIO AMP & JCAK  
 40\_USB CONN  
 41\_BT  
 42\_TPM  
 43\_Debug CONN.  
 44\_EC-IT8510E  
 45\_Touch Pad & KB  
 46\_ISA ROM  
 47\_SWITCH  
 48\_LED  
 49\_THER SENSOR & FAN  
 50\_DC & BAT IN  
 51\_DISCHARGE  
 52\_SREW HOLE  
 53\_EMI  
 54\_POWER\_FLOWCHART  
 55\_POWER\_CHARGER  
 56\_POWER\_VCORE  
 57\_POWER\_SYSTEM  
 58\_POWER\_1.5V&1.8VSB&VCCP&1.9V  
 59\_POWER\_VTT\_DDR&5VLCM&PG\_DT&3VA  
 60\_POWER\_LOAD SWITCH



EC GPIO SETTING

Pin	Pin Name	Signal Name	Type	Default	EC Default
32	PWM0/GPA0	/			GPI
33	PWM1/GPA1	FAN_PWM	O	H	GPI
36	PWM2/GPA2	CLK_PWRSV#	O	H	GPI
37	PWM3/GPA3	/	I		GPI
38	PWM4/GPA4	CHG_LED_UP#	O	H	GPI
39	PWM5/GPA5	PWR_LED_UP#	O	H	GPI
40	PWM6/GPA6	/	O		GPI
43	PWM7/GPA7	LCD_BACKOFF#	O	H	GPI
153	RXD/GPB0	NUM_LED	O	L	GPI
154	TXD/GPB1	CAP_LED	O	L	GPI
162	GPB2	SCRLED	O	L	GPI
163	SMCLK0/GPB3	SMB0_CLK	SMCLK0		GPI
164	SMDAT0GPB4	SMB0_DAT	SMDAT0		GPI
5	GA20/GPB5	A20GATE	GA20		GPO
6	KBRST#GPB6	RC_IN#	KBRST#		KBRST#
165	GPB7	/	I		GPI
47	CLKOUT/GPC0	/	O		GPI
169	SMCLK1/GPC1	SMB1_CLK	SMCLK1		GPI
170	SMDAT1/GPC2	SMB1_DAT	SMDAT1		GPI
171	GPC3	MAIL_LED	O	L	GPI
172	TMRI0/WUI2/GPC4	AC_OK#	I		GPI
175	GPC5	OP_SD#	O	H	GPI
176	TMRI1/WUI3/GPC6	BAT_IN_OC#	I	H	GPI
1	CK32KOUT/GPC7	/			GPI
26	R11#WUI0/GPD0	SUSB#	I		GPI
29	R12#WUI1/GPD1	SUSC#	I		GPI
30	LPCRST#WUI4/GPD2	PLT_RST#	LPCRST		LPCRST
31	ECSC#GPD3	EXT_SC#	ECSC#	H	GPI
41	GPD4	RF_ON_SW#	O	H	GPI
42	GINT/GPD5	/			GPI
62	TACH0/GPD6	FAN0_TACH	TACH0		GPI
63	TACH1/GPD7	/			GPI
87	ADC4/GPE0	DISTP_SW#	I		GPI
88	ADC5/GPE1	/			GPI
89	ADC6/GPE2	EMAIL_SW#	I		GPI
90	ADC7/GPE3	EXPLORE_SW#	I		GPI
2	PWRSW/GPE4	PWR_SW#	PWRSW		GPI
44	WUI5/GPE5	/			GPI
24	LPCPD#WUI6/GPE6	LID_EC#	I		GPI
25	CLKRUN#WUI7/GPE7	/			GPI
110	PS2CLK0/GPF0	/			GPI
111	PS2DAT0/GPF1	/			GPI
114	PS2CLK1/GPF2	/			GPI
115	PS2DAT1/GPF3	/			GPI
116	PS2CLK2/GPF4	TP_CLK	PS2CLK2		GPI
117	PS2DAT2/GPF5	TP_DAT	PS2DAT2		GPI
118	PS2CLK3/GPF6	/			GPI
119	PS2DAT3/GPF7	INTERNET#	I		GPI
113	FA16/GPG0	FA16	FA16		GPI
112	FA17/GPG1	FA17	FA17		GPI
104	FA18/GPG2	FA18	FA18		GPI
103	FA19/GPG3	/			GPI
3	FA20/GPG4	THRM_CPU#	I	H	GPI
4	FA21/GPG5	/			GPI
27	LPC80HL/GPG6	PMTHERM#	O	H	GPI
28	LPC80LL/GPG7	AC_APP_UC#	I	H	GPI

Pin	Pin Name	Signal Name	Type	Default
48	GPH0	VSUS_ON	O	L
54	GPH1	VSUS_GD#	I	H
55	GPH2	CPUPWR_GD#	I	H
69	GPH3	PM_PWRBTN#	O	H
70	GPH4	SUSC_ON	O	L
75	GPH5	SUSB_ON	O	L
76	GPH6	CPU_VRON	O	L
105	GPH7	PM_RSMRST#	O	L
148	GPI0	ICH7_PWROK	O	L
149	GPI1	/	O	
152	GPI2	MCHOK	I	L
155	GPI3	CHG_EN#	O	H
156	GPI4	PRECHG	O	L
168	GPI5	BAT_LL#	O	H
174	GPI6	BAT_LEARN	O	L
93	ADC8	KID0	I	
94	ADC9	KID1	I	
101	DAC2	BL_PWM_DA	O	
102	DAC3	BATSEL_2P#	O	

06/01/23

SM-Bus Device	SM-Bus Address
Clock Generator	1101001x ( D2 )
SO-DIMM 0	1010000x ( A0 )
SO-DIMM 1	1010001x ( A2 )
Thermal Sensor	01001100 ( 4C )

PCI Device	IDSEL#	REQ/GNT#	Interrupts
CARD READER	AD24	0	C
1394	AD24	0	B
LAN	AD23	1	D

ICH7-M GPIO SETTING

Pin	Pin Name	Signal Name	Type	Power_Well	Default
AB18	GPIO00/BM_BUSY#	PM_BMBUSY#	I	Core(To:3.3V)	GPI
C8	GPIO01/REQ5#	PCI_REQ#5	I/O	Core(To:5V)	GPI
G8	GPIO02/PIRQE#	PCI_INTE#	I(OD)	Core(To:5V)	GPI
F7	GPIO03/PIRQ#	PCI_INTF#	I(OD)	Core(To:5V)	GPI
F8	GPIO04/PIRQG#	PCI_INTG#	I(OD)	Core(To:5V)	GPI
G7	GPIO05/PIRQH#	PCI_INTH#	I(OD)	Core(To:5V)	GPI
AC21	GPIO06	NC	I/O	Core(To:3.3V)	GPI
AC18	GPIO07	WLAN_BT_LED_ENH#		Core(To:3.3V)	GPI
E21	GPIO08	EXTSM#	I	SUS(To:3.3V)	GPI
E20	GPIO09	SATA_DET#0	I/O	SUS(To:3.3V)	GPI
A20	GPIO10	WLAN_ON#	O	SUS(To:3.3V)	GPI
B23	SMBALERT#GPIO11	SMB_ALERT#	I/O	SUS(To:3.3V)	Native
F19	GPIO12	KBC_SC#	I	SUS(To:3.3V)	GPI
E19	GPIO13	TP	I/O	SUS(To:3.3V)	GPI
R4	GPIO14	NC	I/O	SUS(To:3.3V)	GPI
E22	GPIO15	CB_SD#	I/O	SUS(To:3.3V)	GPI
AC22	GPIO16/DPRSLPVR	PM_DPRSLPVR	O	Core(To:3.3V)	Native
D8	GPIO17/GNT5#	PCI_GNT#5	I/O	Core(To:3.3V)	GPO
AC20	GPIO18/STP_PC#	STP_PC#	O	Core(To:3.3V)	GPO
AH18	GPIO19/SATA1GP	NC	O	Core(To:3.3V)	GPI
AF21	GPIO20/STP_CPU#	STP_CPU#	O	Core(To:3.3V)	GPO
AE19	GPIO21/SATA0GP	NC	I/O	Core(To:3.3V)	GPI
A13	GPIO22/REQ4#	PCI_REQ#4	I/O	Core(To:3.3V)	Native
AA5	LDRQ1#GPIO23	TP	I/O	Core(To:3.3V)	Native
R3	GPIO24	NC	I/O	SUS(To:3.3V)	GPO
D20	GPIO25	NC	I/O	SUS(To:3.3V)	GPO
A21	GPIO26/EL_RSVD	NC	I/O	SUS(To:3.3V)	GPO
B21	GPIO27/EL_STATE0	PD_DET#	I/O	SUS(To:3.3V)	GPO
E23	GPIO28/EL_STATE1	NC	I/O	SUS(To:3.3V)	GPO
C3	GPIO29/OC#5	USB_OC#5	I/O	SUS(To:3.3V)	Native
A2	GPIO30/OC#6	NEWCARD_OC#	I	SUS(To:3.3V)	Native
B3	GPIO31/OC#7	USB_OC#7	I/O	SUS(To:3.3V)	Native
AG18	GPIO32/CLKRUN#	PM_CLKRUN#	O	Core(To:3.3V)	GPO
AC19	GPIO33/AZ_DOCK_EN#	BT_ON#	O	Core(To:3.3V)	GPO
U2	GPIO34/AZ_DOCK_RST#	NC	I/O	Core(To:3.3V)	GPO
AD21	GPIO35	NC	I/O	Core(To:3.3V)	GPO
AH19	GPIO36/SATA2GP	NC	I/O	Core(To:3.3V)	GPI
AE19	GPIO37/SATA3GP	PCB_ID0	I	Core(To:3.3V)	GPI
AD20	GPIO38	PCB_ID1	I	Core(To:3.3V)	GPI
AE20	GPIO39	PCB_ID2	I	Core(To:3.3V)	GPI
A14	GNT4#GPIO48	PCI_GNT#4	I/O	Core(To:3.3V)	Native
AG24	GPIO49/CPUPWRGD	H_PWRGD	O	V_CPU_IO	Native



### CIRCUIT UPDATED HISTORY

Rev	Date	Description
1.00G	2006/03/06	Z96H Schematic 1.00G (base on Z96F), NB: SiS M662MX SB: SiS 966L

Rev	Date	Description



<http://hobi-elektronika.net>

ASUS <sup>®</sup>		Title : Blank	
ASUSTeK COMPUTER INC		Engineer: Kell Huang	
Size	Project Name		Rev
A3	Z96H		1.00G
Date: Wednesday, May 17, 2006		Sheet	5 of 60

	5	4	3	2	1
D					
C					
B					
A					
	5	4	3	2	1

A



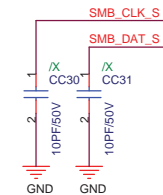
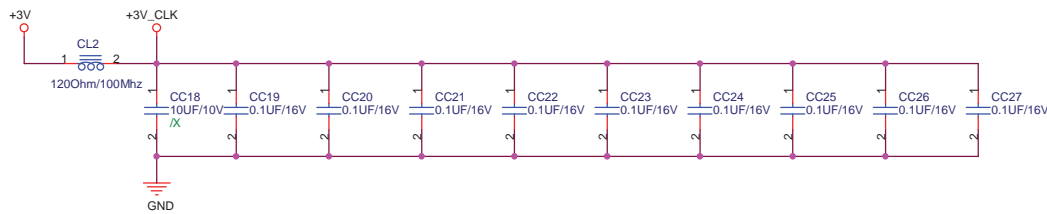
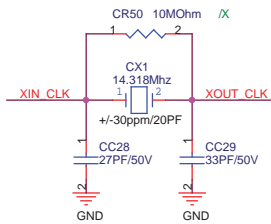
Title :  
Blank

Engineer: *Kell Huang*

Size	Project Name	Rev
A3	<b>Z96H</b>	1.00G

Date: Wednesday, May 17, 2006

Sheet 6 of 60



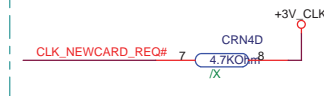
### CLK\_MODE

0 = Desktop Mode

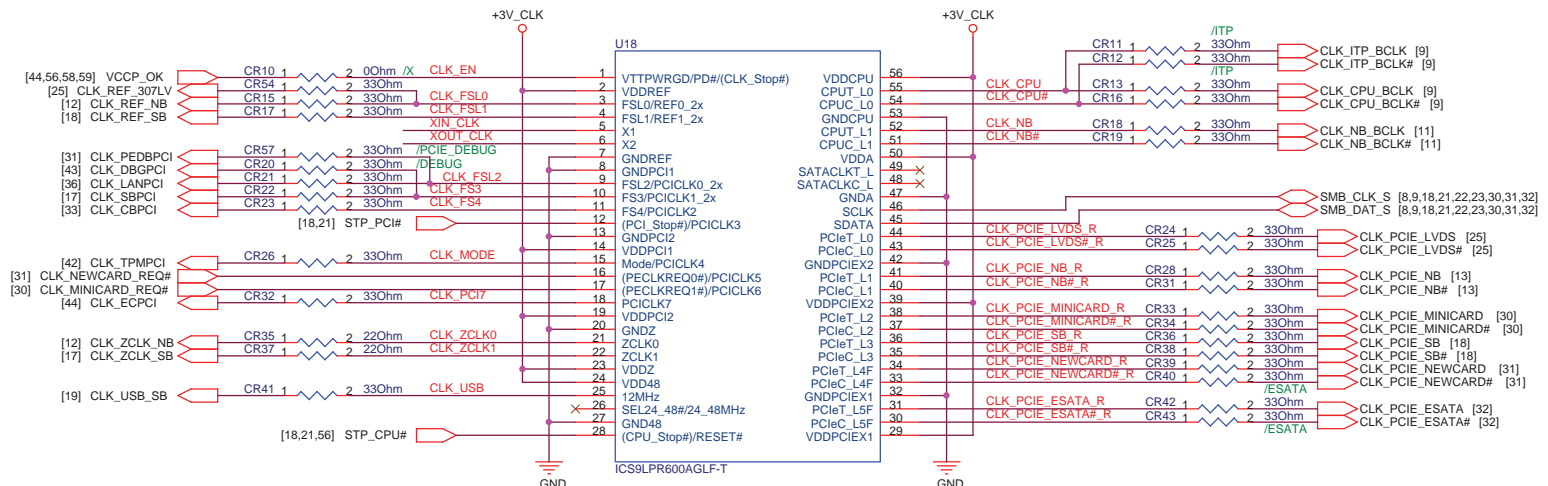
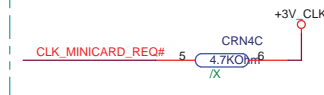
1 = Mobile Mode



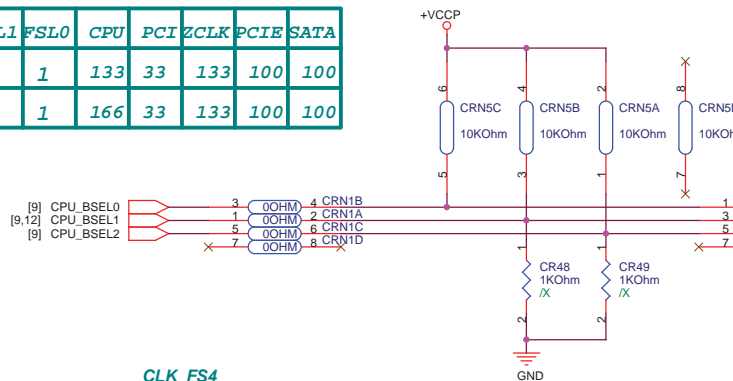
### PEREQ0# control PCIE 0/1/4



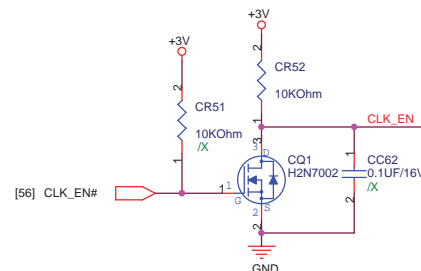
### PEREQ1# control PCIE 2/3/5



FS4	FS3	FSL2	FSL1	FSL0	CPU	PCI	ZCLK	PCIE	SATA
0	1	0	0	1	133	33	133	100	100
0	1	0	1	1	166	33	133	100	100



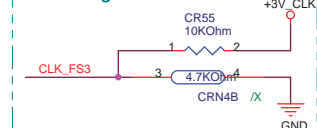
BCLK	FSB	BSEL2	BSEL1	BSEL0
133	533	L	L	H
166	667	L	H	H



### CLK\_FS3

0 = FS3 Low Level

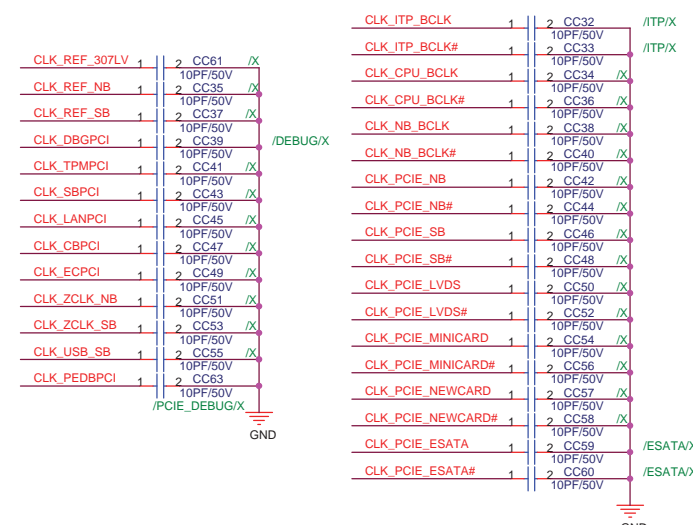
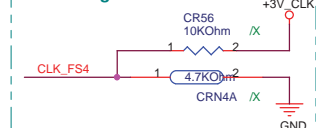
1 = FS3 High Level



### CLK\_FS4

0 = FS4 Low Level

1 = FS4 High Level

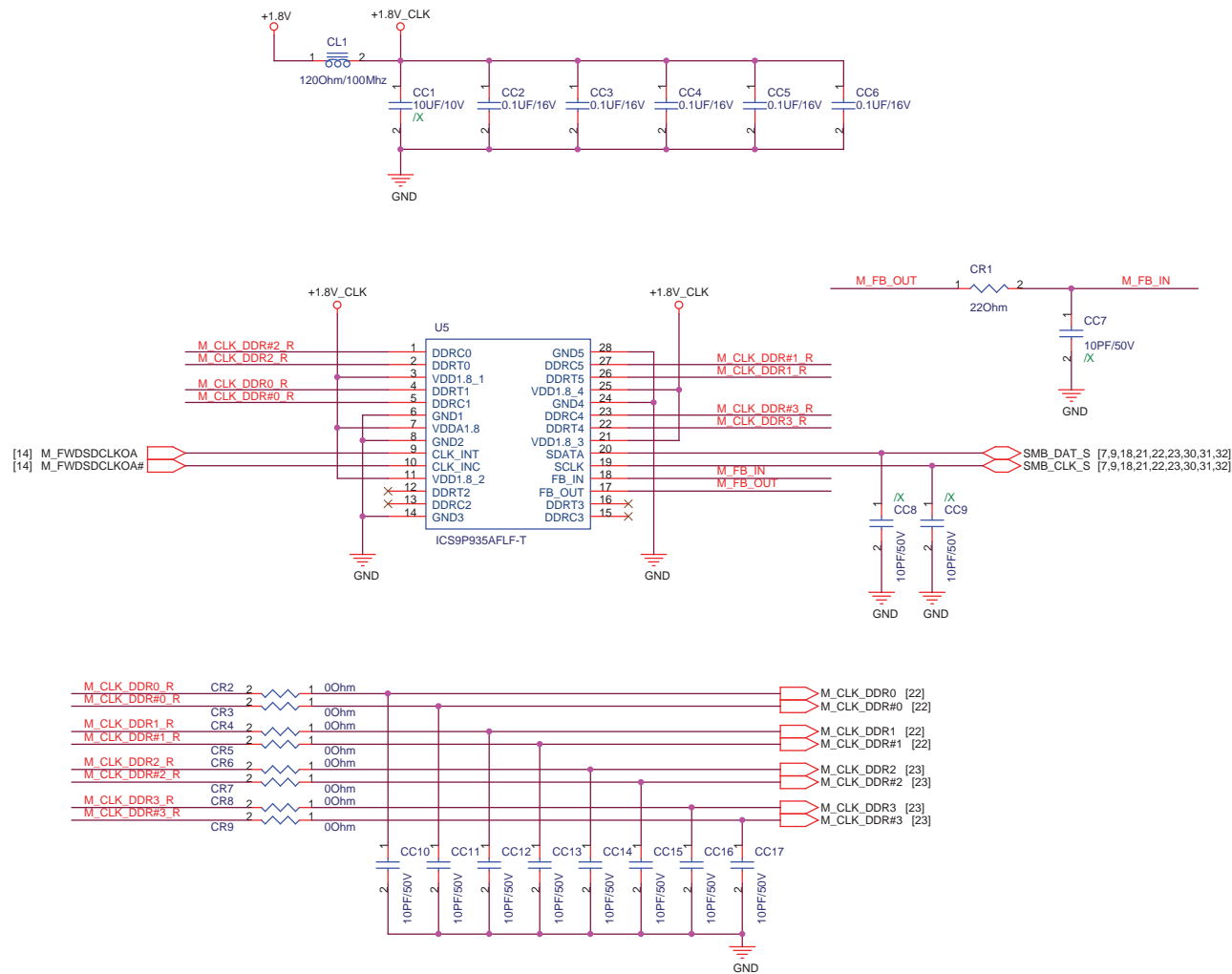


**ASUS** Title :CLOCK GEN-ICS9LPR600

ASUSTeK COMPUTER INC. Engineer: Kell Huang

Size A3 Project Name **Z96H** Rev 1.00G

Date: Wednesday, May 17, 2006 Sheet 7 of 60

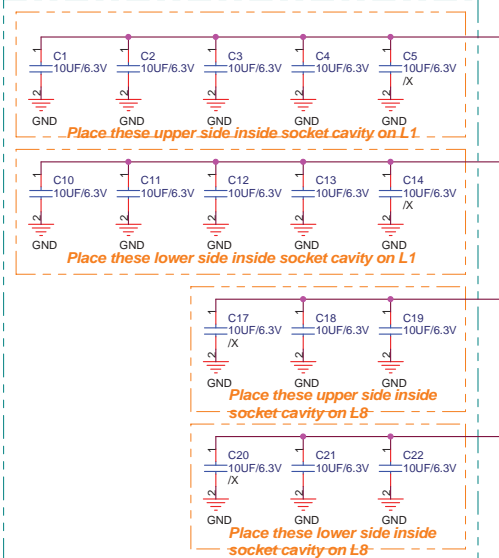






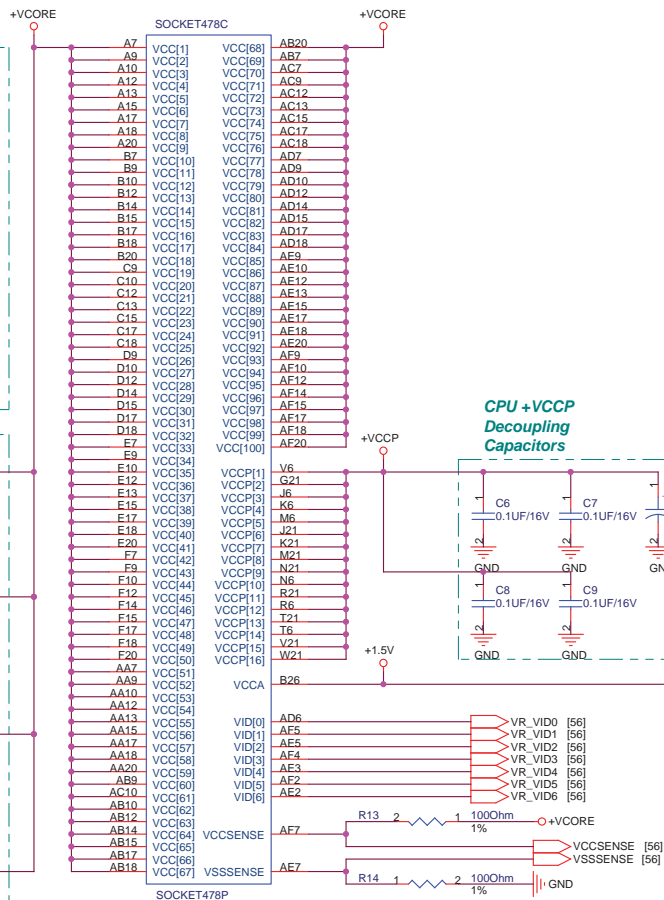
**CPU +VCORE  
Bulk-Decoupling  
Capacitors**

**CPU +VCORE  
Mid-Frequency  
Capacitors**



**+VCORE Mid-Frequency Capacitor**  
Intel: 220UF \*32  
R1F: 10UF \*16

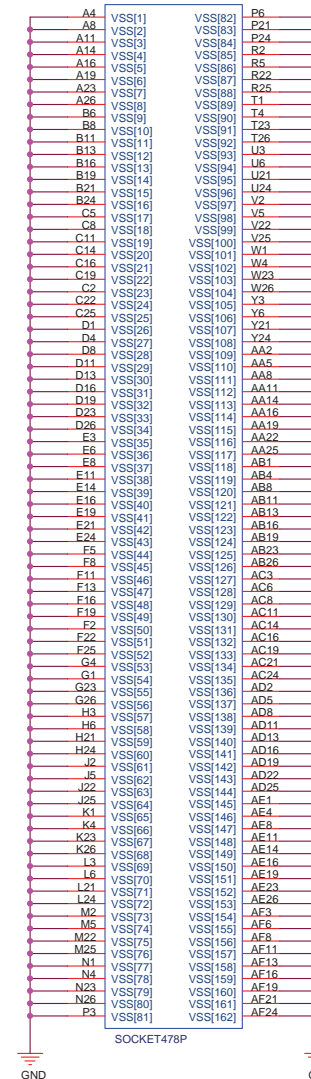
**+VCCP Decoupling Capacitor**  
Intel: 270UF \*1, 0.1UF \*6  
R1F: 220UF \*1, 0.1UF \*4



**CPU +VCCP  
Decoupling  
Capacitors**

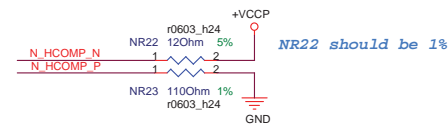
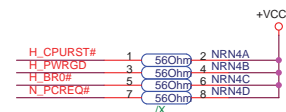
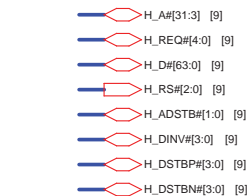
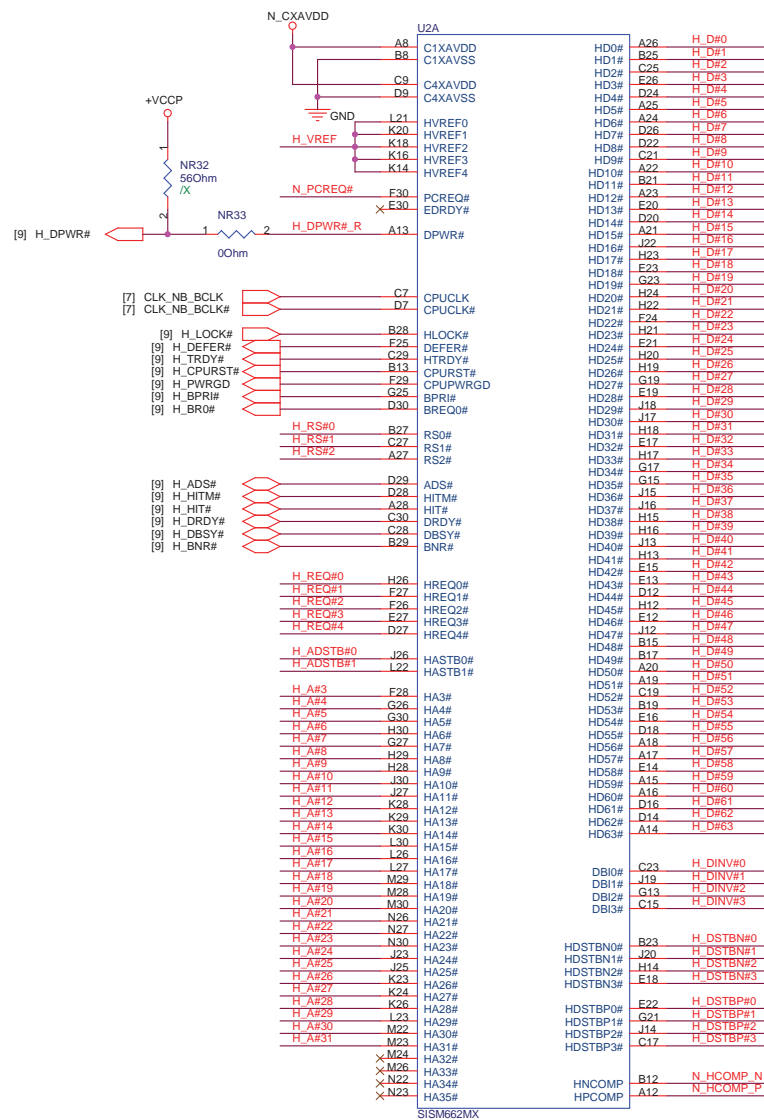
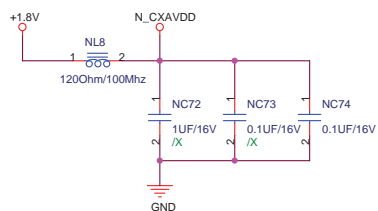
**CPU +VCCA  
Decoupling  
Capacitors**

SOCKET478D

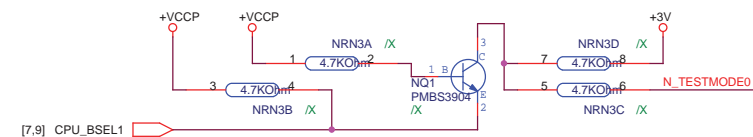
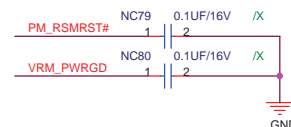
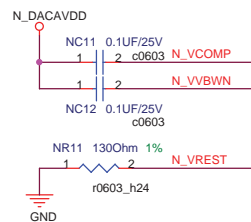
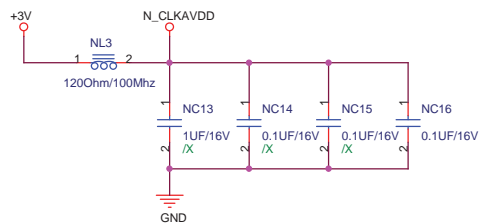


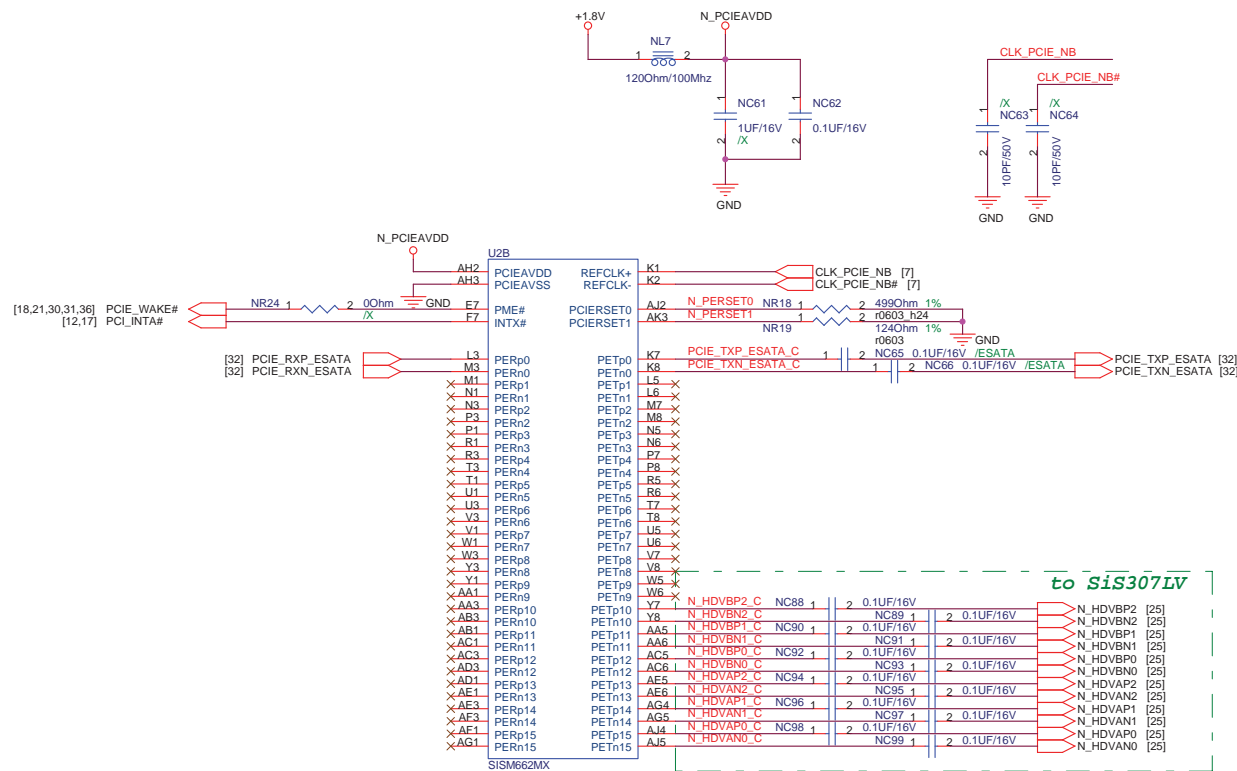
The schematic diagram shows the input stage of the ADXL05. It features a differential input stage with two resistors, NR20 and NR21, connected to +VCCP and GND. The resistors are 750 Ohm and 150 Ohm, respectively, with 1% tolerance. The circuit includes three capacitors: NC67 (0.1 uF/16V), NC68 (0.1 uF/16V), and NC69 (0.01 uF/16V). The output is connected to H\_VREF.

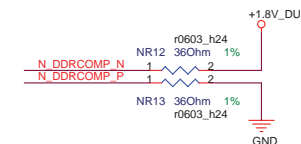
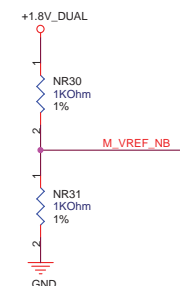
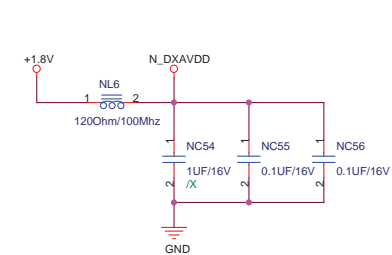
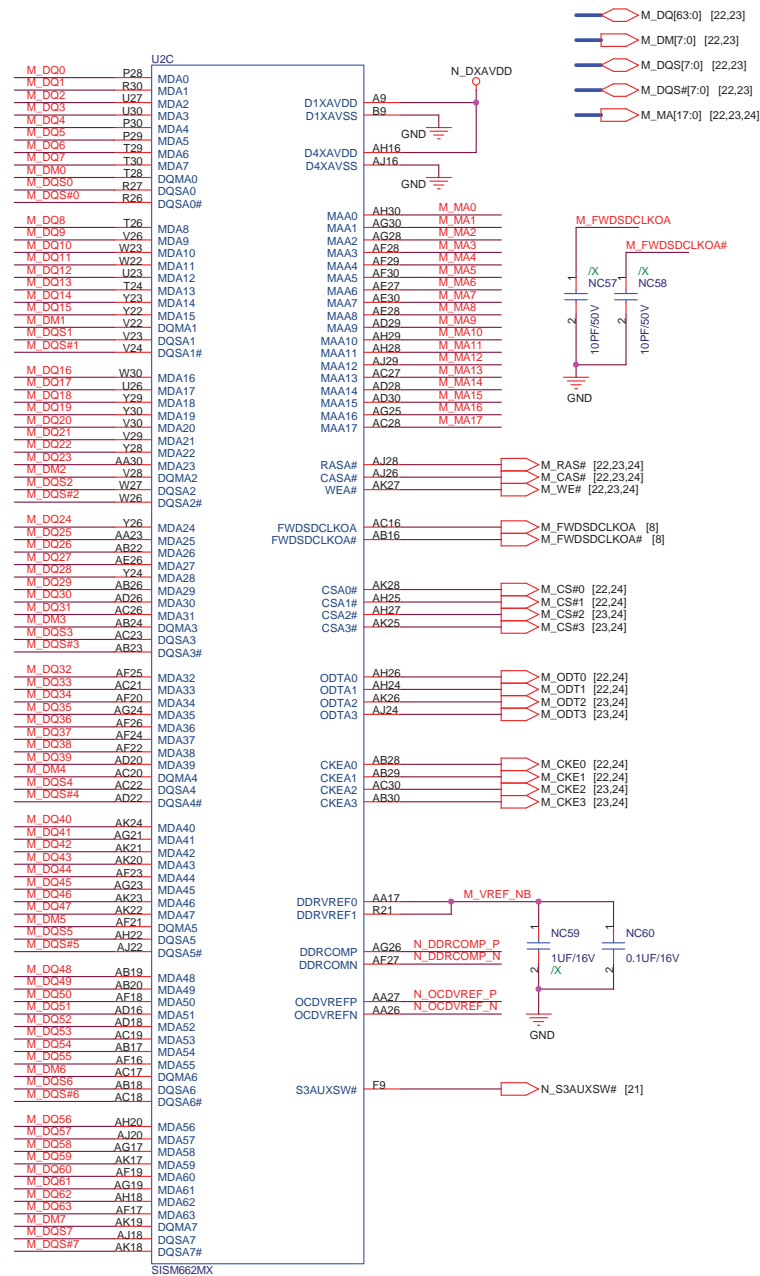
The diagram shows two digital signals, CLK\_NB\_BCLK (red) and CLK\_NB\_BCLK# (red), connected to two inverters, NC70 and NC71, respectively. Both inverters are powered by a 10PF/50V capacitor connected to GND. The signals are shown as square waves, with CLK\_NB\_BCLK# being the inverted version of CLK\_NB\_BCLK.



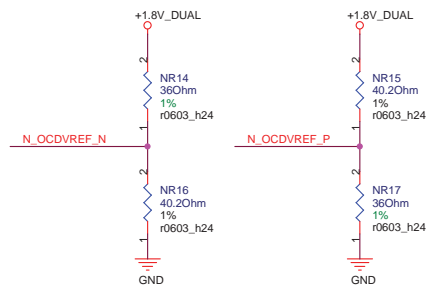
Trace should be 10 mil wide  
with 20 mil spacing

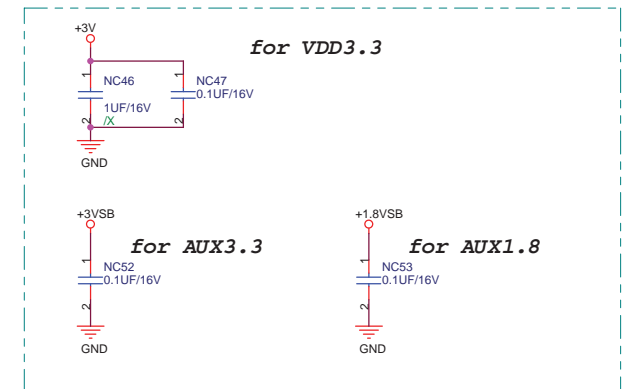
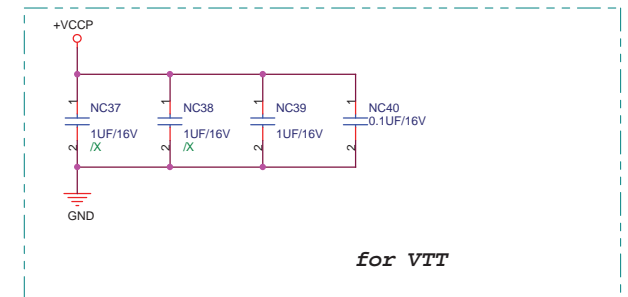
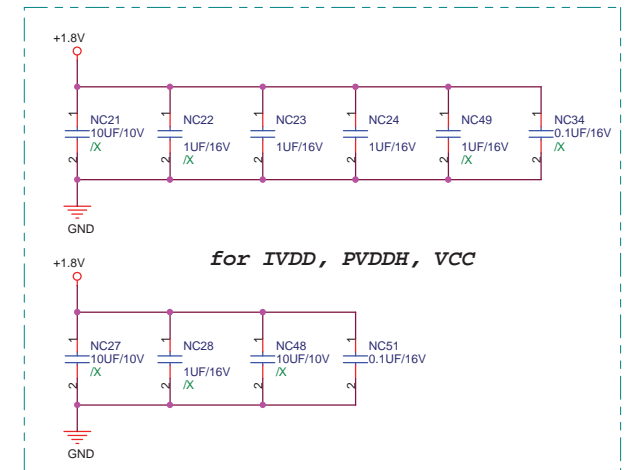
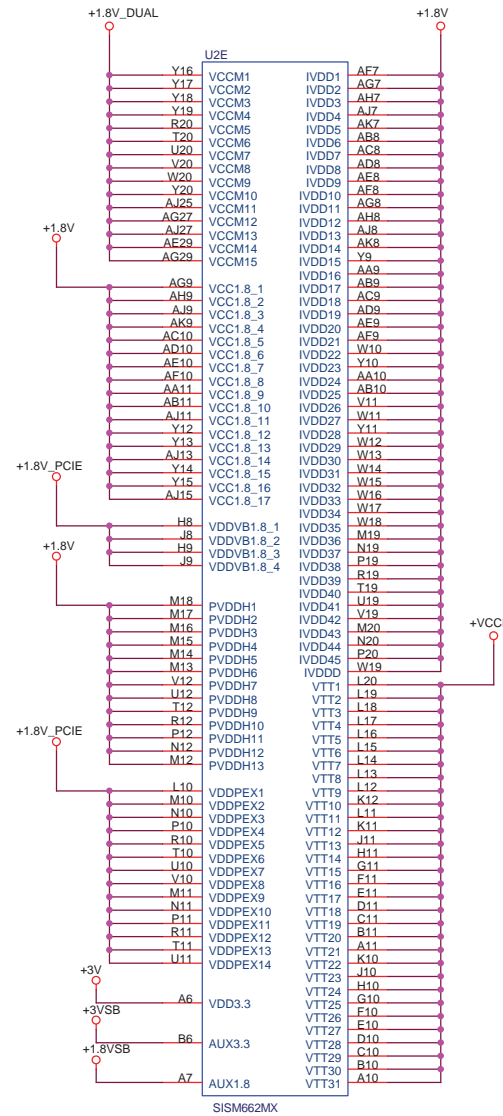
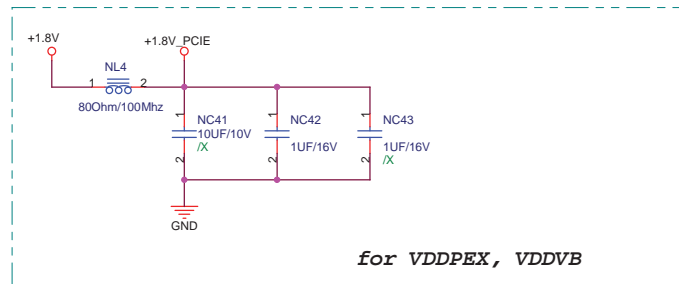
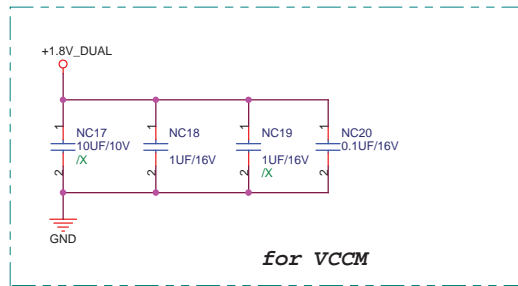






Layout Note:  
Route as short as possible

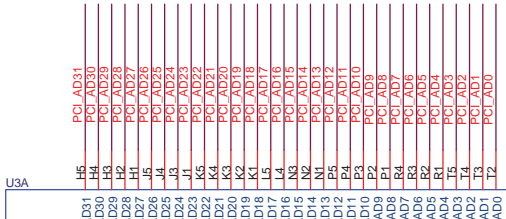
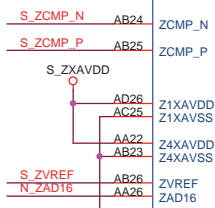
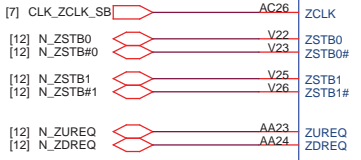
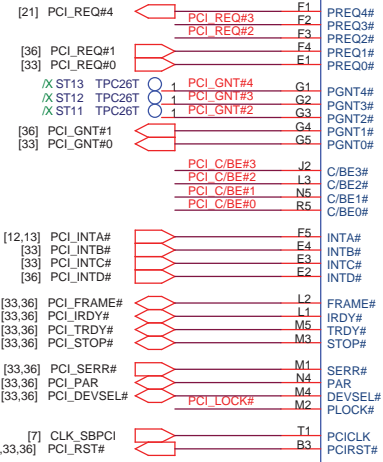
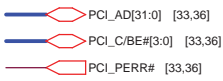
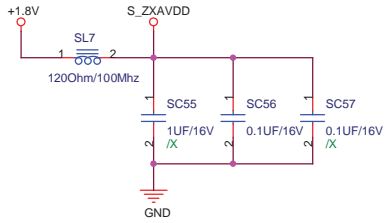
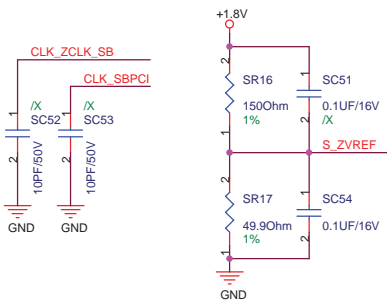
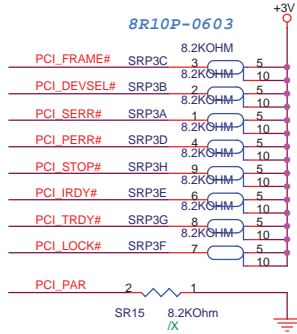
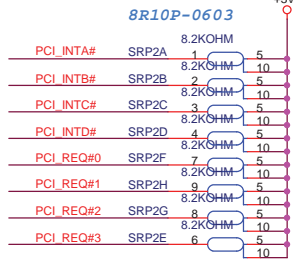




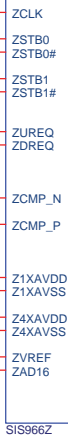




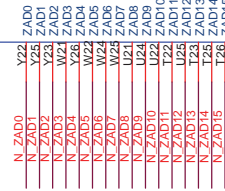




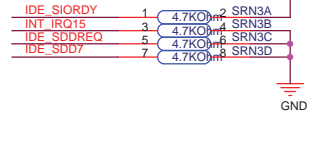
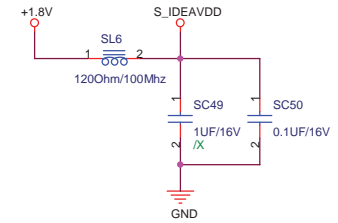
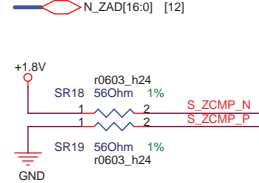
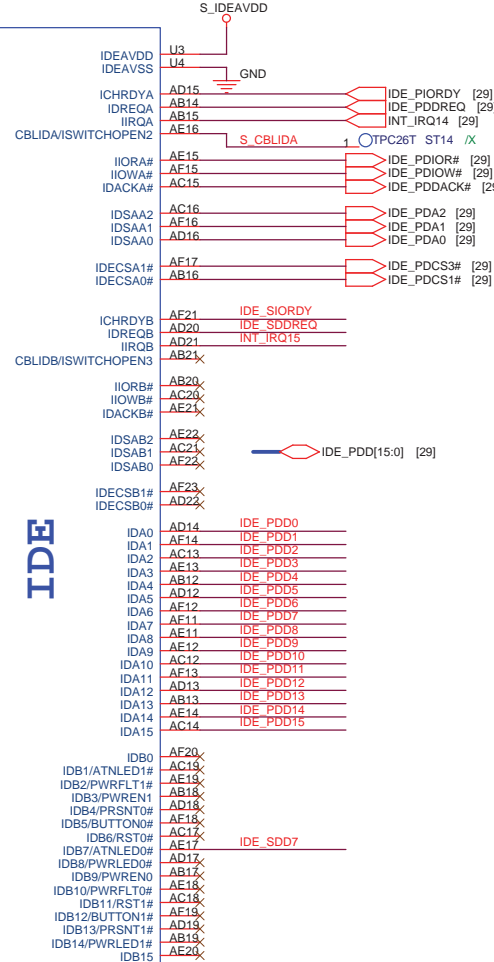
PCI

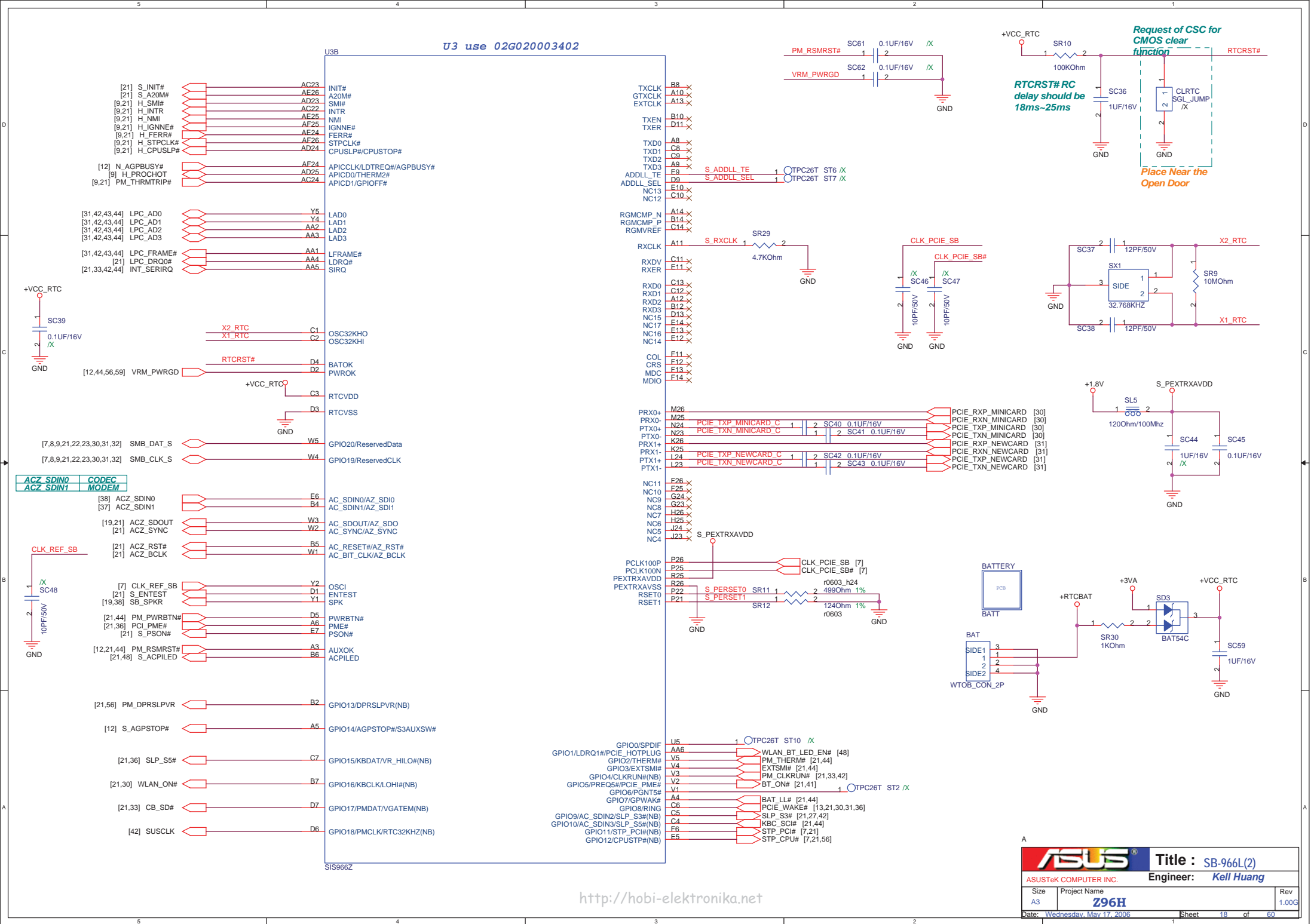


MuTIOL



U3 use 02G020003402





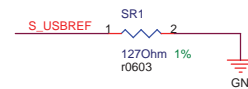
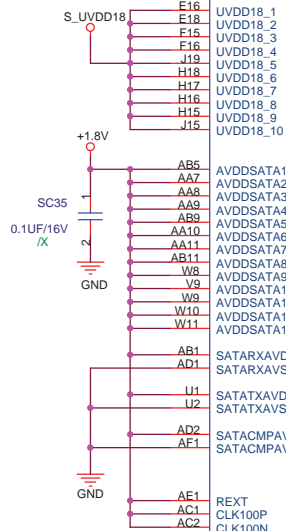


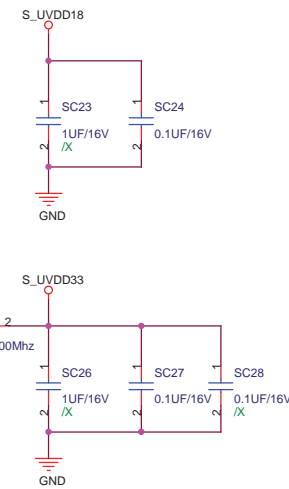
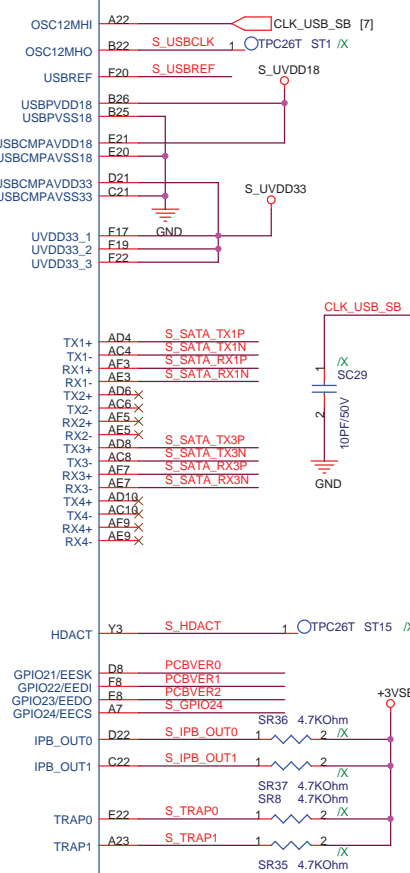
Figure 10: USB to UART bridge connection diagram. This diagram shows the internal connections of the USB to UART bridge. On the left, USB pins are listed: [40] USB\_PP0, [40] USB\_PN0, [40] USB\_PP1, [40] USB\_PN1, [40] USB\_PP2, [40] USB\_PN2, [40] USB\_PP3, [40] USB\_PN3, [41] USB\_PP4, and [41] USB\_PN4. On the right, UART pins are listed: UV0+, UV0-, UV1+, UV1-, UV2+, UV2-, UV3+, UV3-, UV4+, UV4-, UV5+, UV5-, UV6+, UV6-, UV7+, and UV7-. In the center, internal bridge pins are listed: D26, D25, E24, E23, A20, B20, C19, A18, B18, C17, D17, A16, B16, C15, and D15. Red lines indicate the connections between the USB pins and the internal bridge pins, and between the internal bridge pins and the UART pins. For example, USB\_PP0 connects to D26, which connects to UV0+. USB\_PN0 connects to D25, which connects to UV0-. USB\_PP1 connects to E24, which connects to UV1+. USB\_PN1 connects to E23, which connects to UV1-. USB\_PP2 connects to A20, which connects to UV2+. USB\_PN2 connects to B20, which connects to UV2-. USB\_PP3 connects to C19, which connects to UV3+. USB\_PN3 connects to A18, which connects to UV3-. USB\_PP4 connects to B18, which connects to UV4+. USB\_PN4 connects to C17, which connects to UV4-. USB\_PP5 connects to D17, which connects to UV5+. USB\_PN5 connects to A16, which connects to UV5-. USB\_PP6 connects to B16, which connects to UV6+. USB\_PN6 connects to C15, which connects to UV6-. USB\_PP7 connects to D15, which connects to UV7+. USB\_PN7 connects to A24, which connects to UV7-. Additionally, USB\_CON\_OC01# connects to F21, which connects to OC0#. USB\_CON\_OC23# connects to A25, which connects to OC2#. USB\_CON\_OC5# connects to B24, which connects to OC3#. USB\_CON\_OC5# also connects to C23, which connects to OC4#. NEWCARD\_OC# connects to C24, which connects to OC5#. NEWCARD\_OC# also connects to A26, which connects to OC6#. NEWCARD\_OC# also connects to B23, which connects to OC7#.



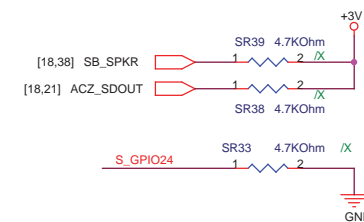
Pin connections for the ADXL345 accelerometer:

- TX Pins:**
  - S\_SATA\_TX1P (Pin 1) → 1KOhm → SRN15A (Pin 4)
  - S\_SATA\_TX1N (Pin 3) → 1KOhm → SRN15B (Pin 4)
  - S\_SATA\_TX3P (Pin 5) → 1KOhm → SRN15C (Pin 4)
  - S\_SATA\_TX3N (Pin 7) → 1KOhm → SRN15D (Pin 4)
- RX Pins:**
  - S\_SATA\_RX1P (Pin 7) → 1KOhm → SRN16D (Pin 4)
  - S\_SATA\_RX1N (Pin 5) → 1KOhm → SRN16C (Pin 4)
  - S\_SATA\_RX3P (Pin 3) → 1KOhm → SRN16A (Pin 4)
  - S\_SATA\_RX3N (Pin 1) → 1KOhm → SRN16B (Pin 4)
- Power:**
  - VCC (Pin 2) → +1.8V
  - GND (Pin 6) → GND

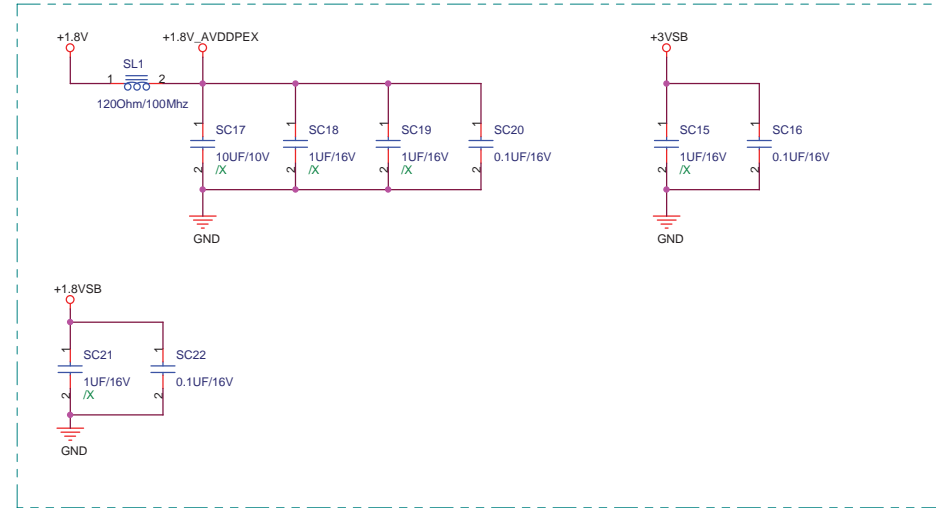
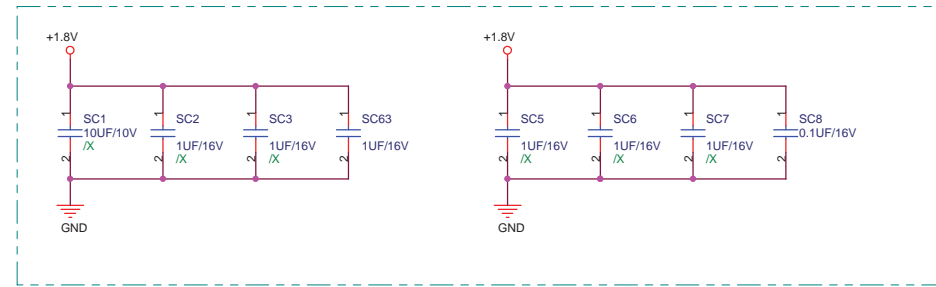
Signal	Description	High	Low	Default
S_TRAP0	MuTIOL Operation Frequency	66MHz	133MHz	Internal pull-down
S_TRAP1	Reserved			Internal pull-down
S_IPB_OUT0	MuTIOL Clock PLL	Disable	Enable	Internal pull-down
S_IPB_OUT1	MuTIOL Version	v1.0	v2.0	Internal pull-down
SB_SPKR	First Flash Memory Cycle Type	Firmware Memory Type	LPC Memory Type	Internal pull-down
ACZ_SDOUT	Trap From	PCI AD	ROM	Internal pull-down
USB_OC#4	SB Debug Mode	Disable	Enable	External pull-up



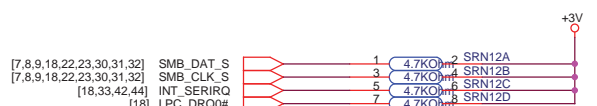
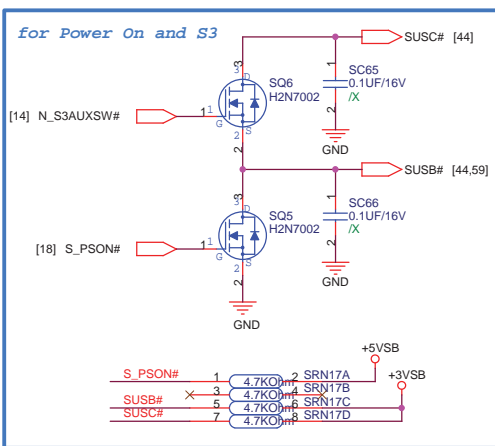
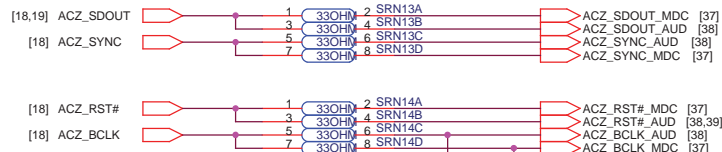
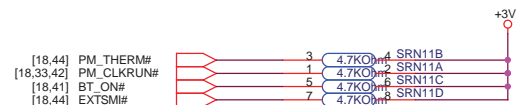
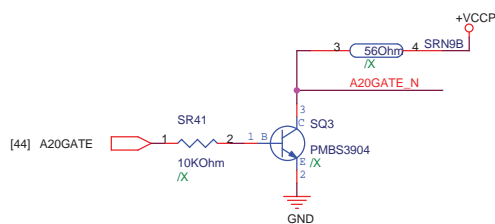
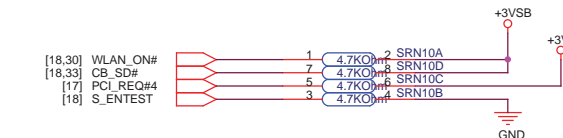
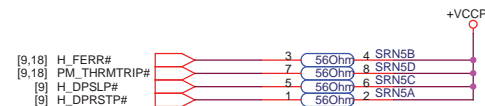
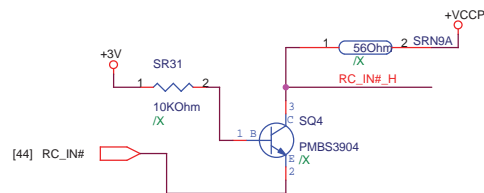
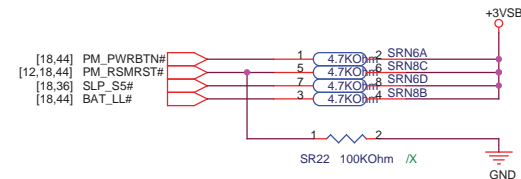
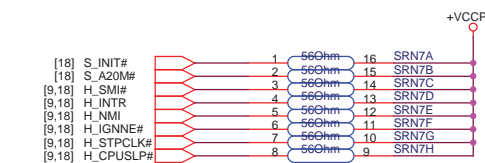
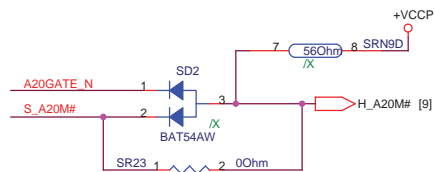
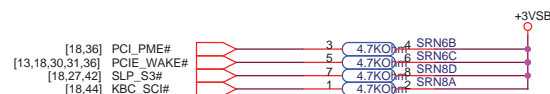
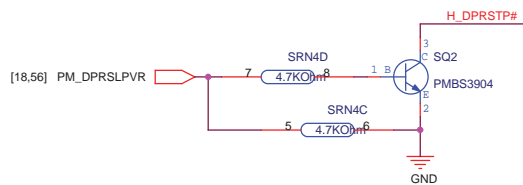
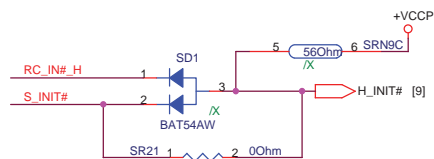
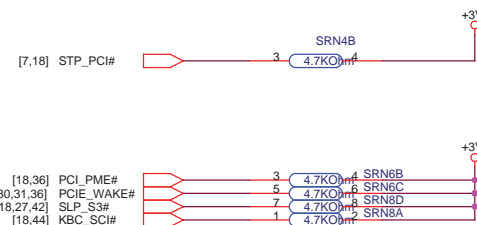
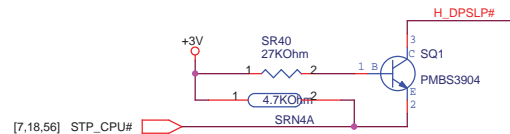
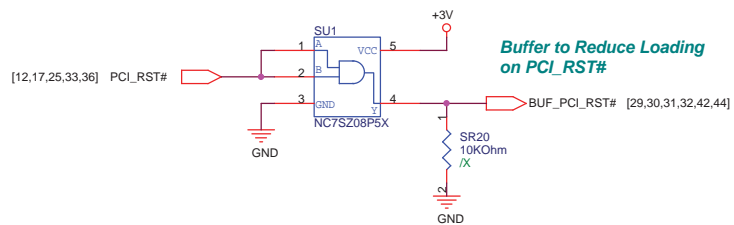
PCB Version



U3 use 02G020003402

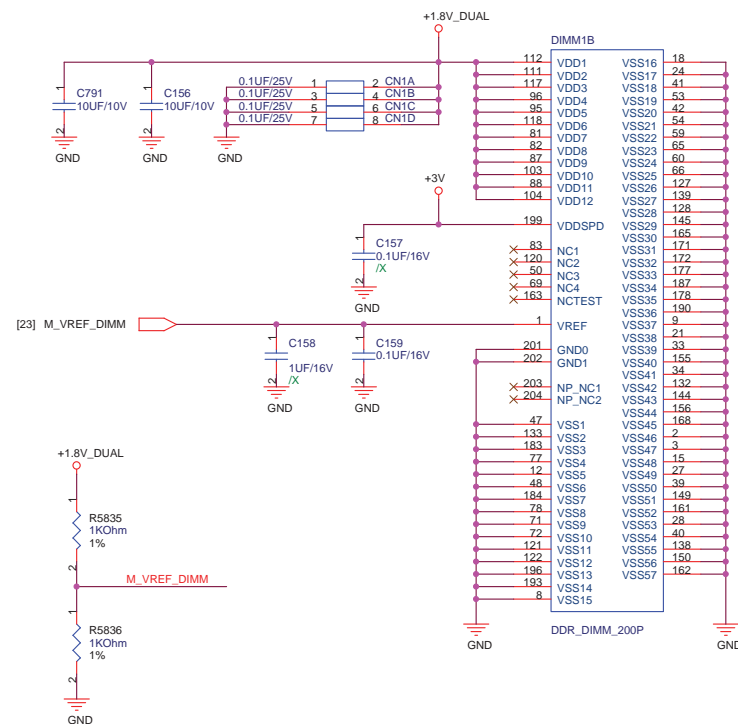
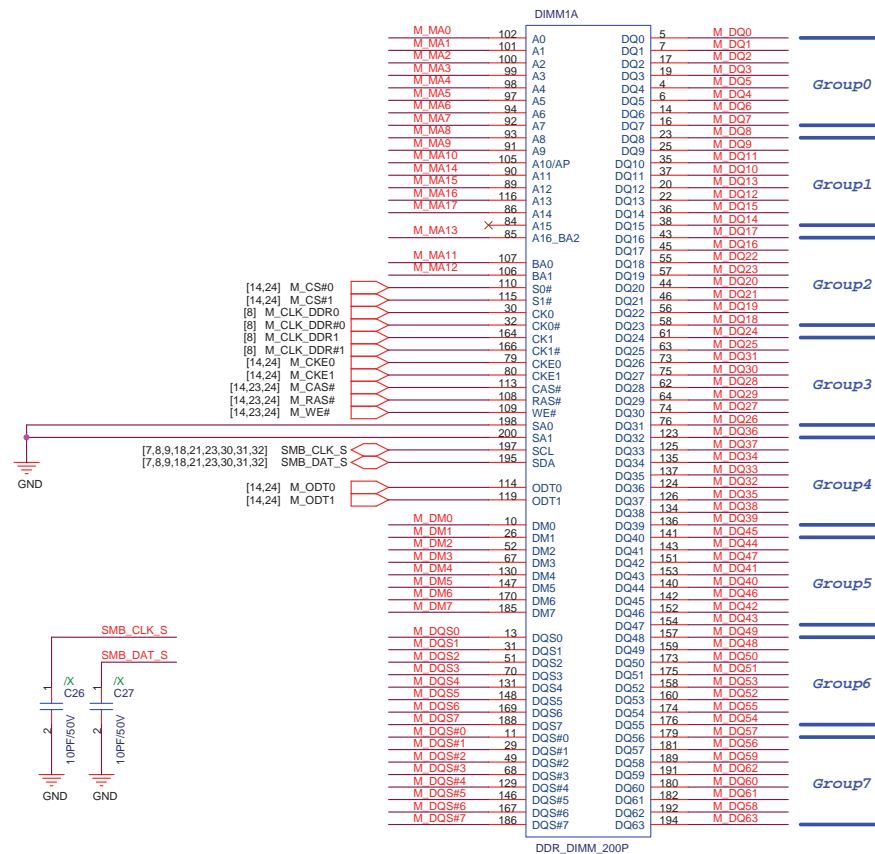


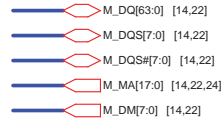
<http://hobi-elektronika.net>



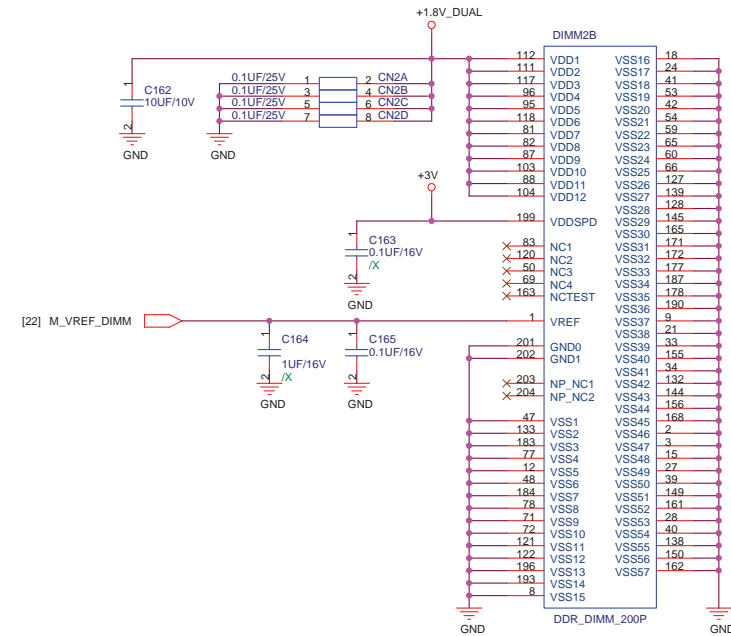
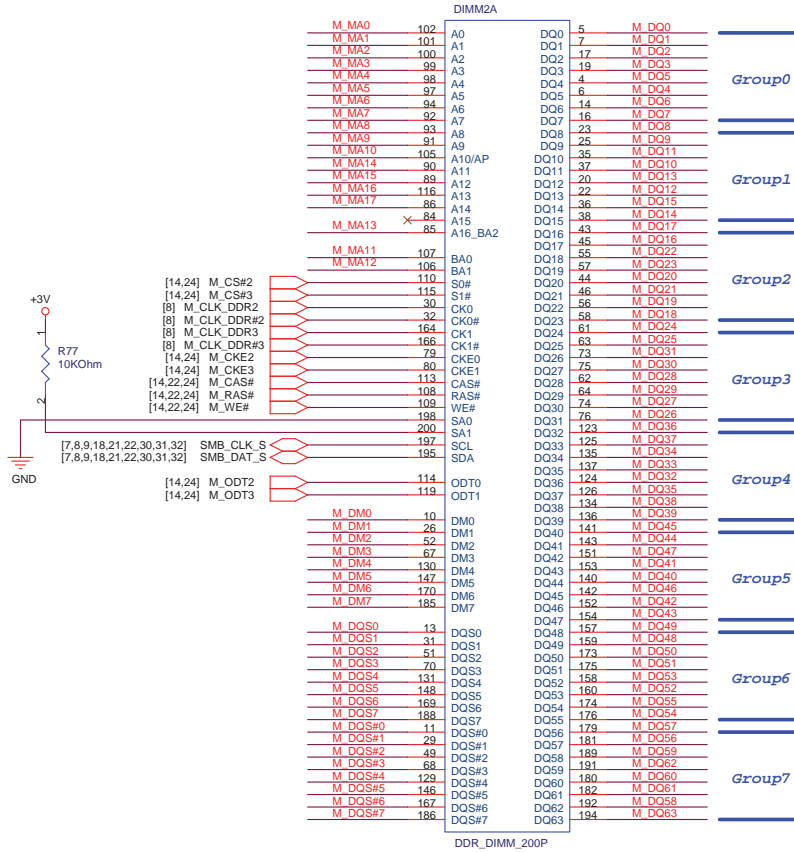
M\_DQ[63:0] [14,23]  
M\_DQS[7:0] [14,23]  
M\_DQS#[7:0] [14,23]  
M\_MA[17:0] [14,23,24]  
M\_DM[7:0] [14,23]

# REV Type

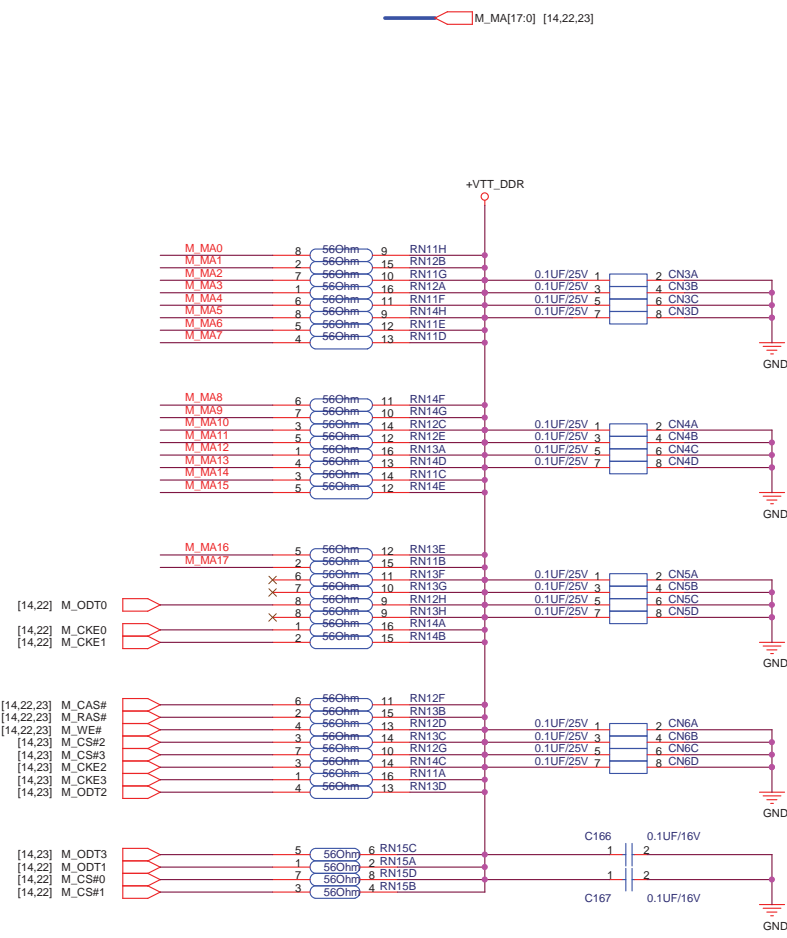




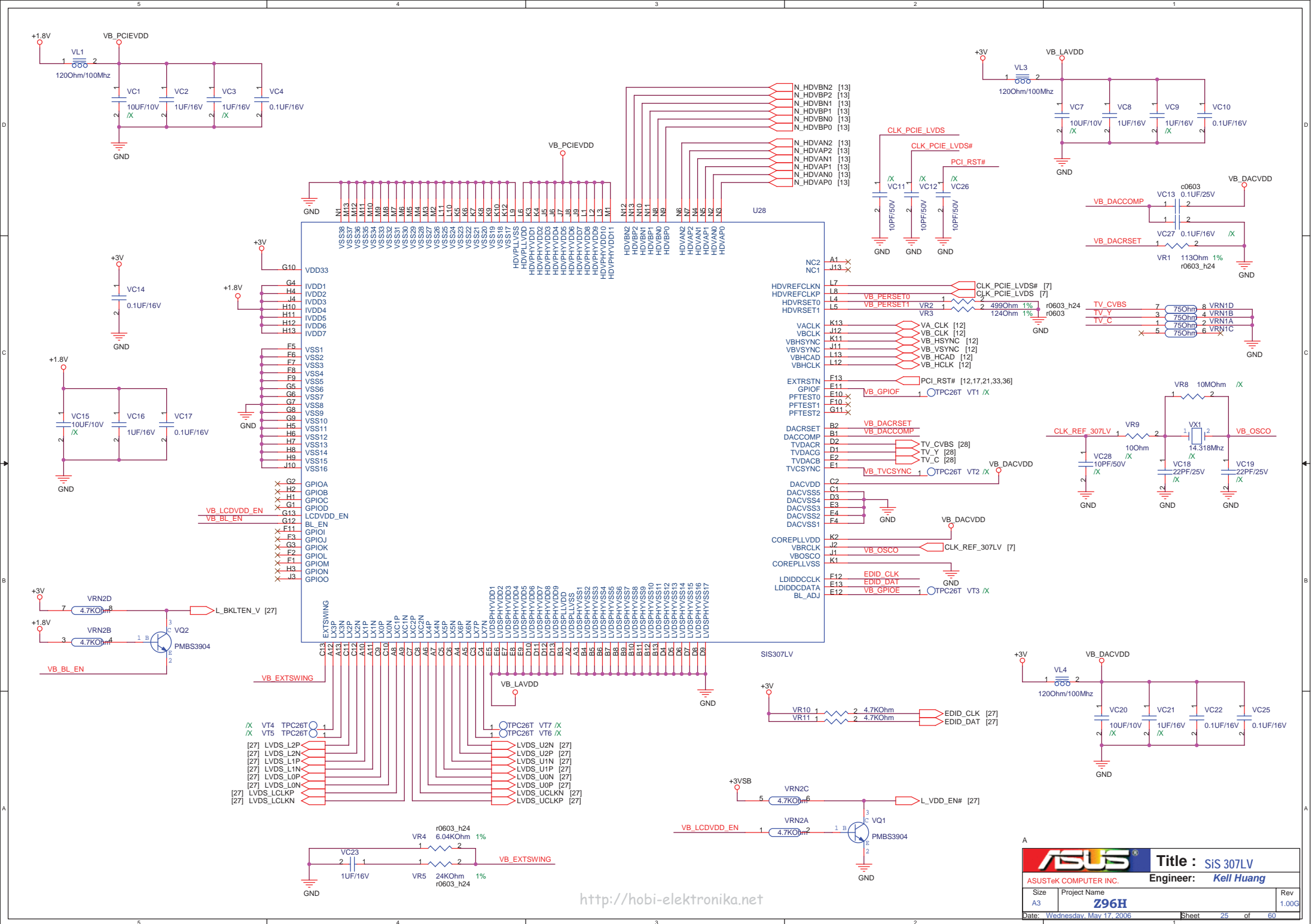
### STD Type











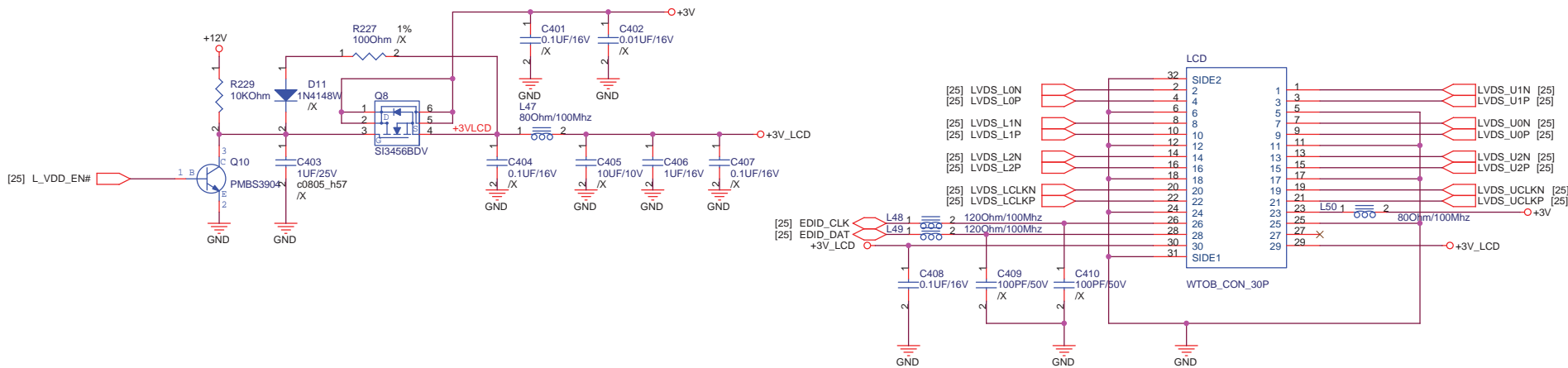


# LCD Backlight Control

## LCD Power

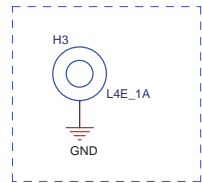
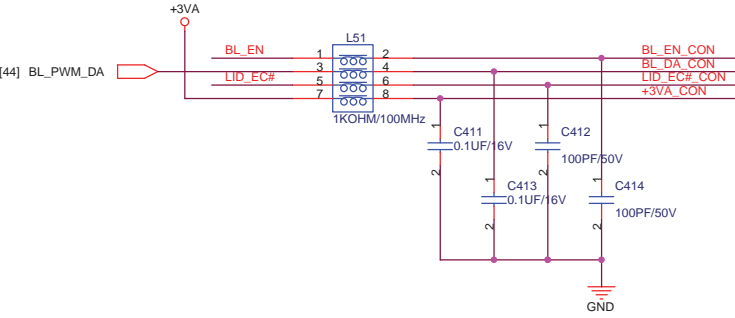
Cable Requirement:  
Impedence: 100 ohm +/- 10%  
Length Mismatch <= 10 mils  
Twisted Pair(Not Ribbon)  
Maximum Length <= 16"

# LCD LVDS Interface

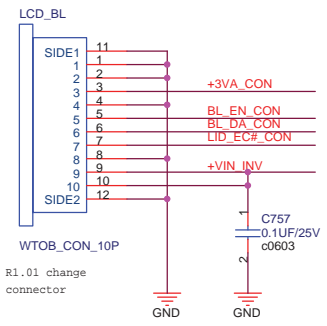
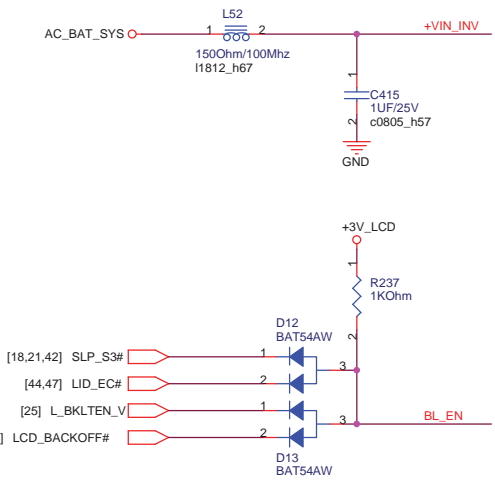


## INVERTER Interface/Speaker CONN.

BIOS  
BACK\_OFF#:When user push "Fn+F7"  
button, BIOS active this pin to  
turn off back light.

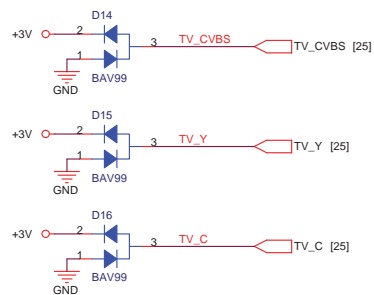


LCD NUT(3.0mm) \*1

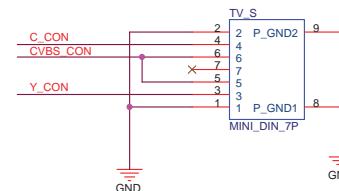
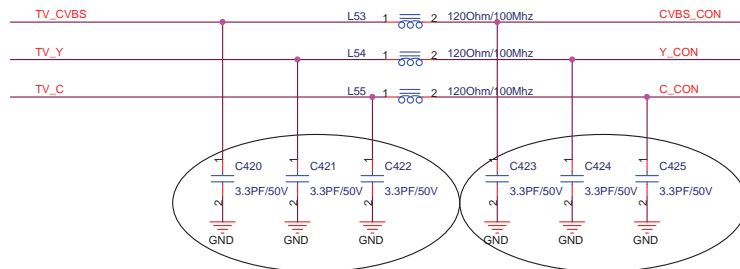


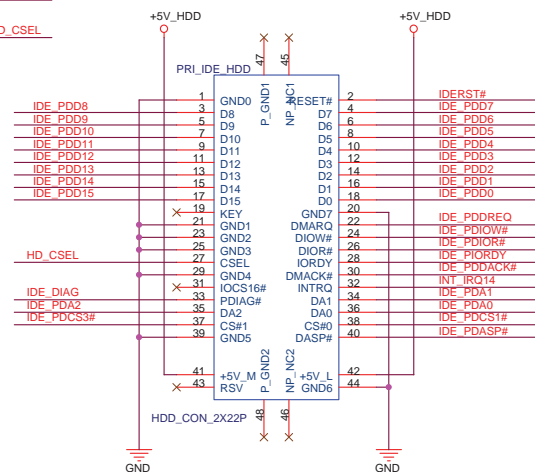
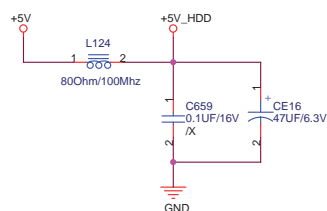
<http://hobi-elektronika.net>

TV  
OUT



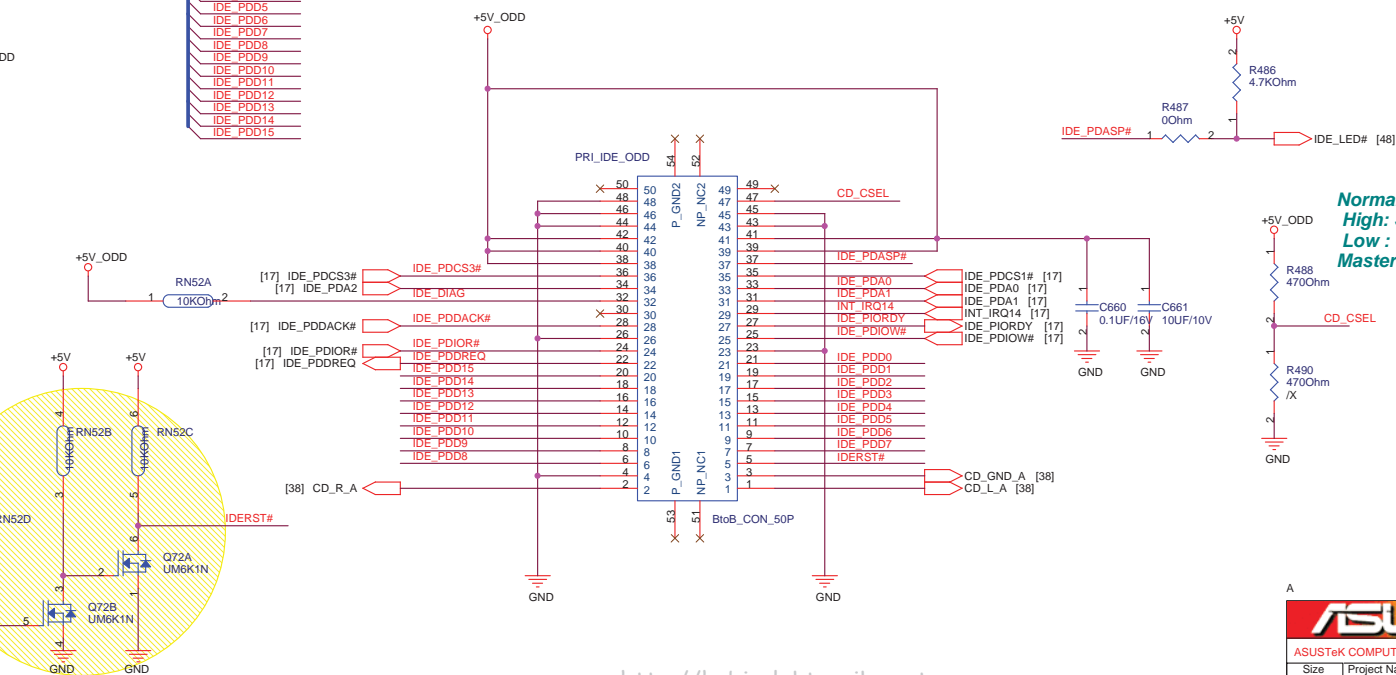
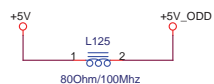
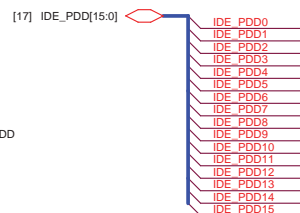
PLACE ESD Diodes near TV port



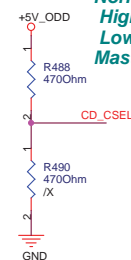


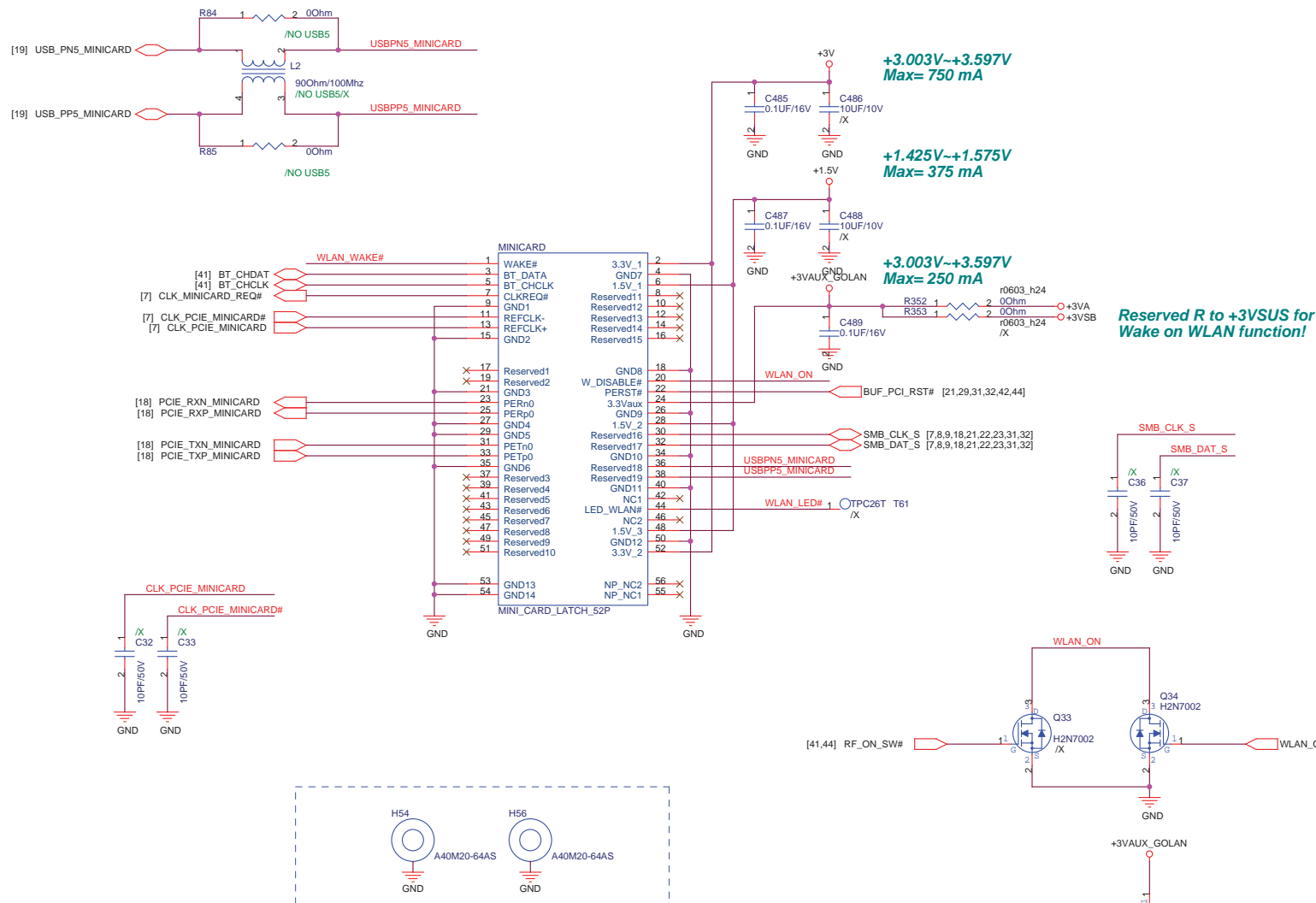
## PATA HDD

**ODD**

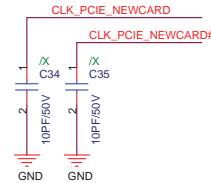
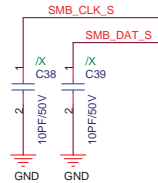
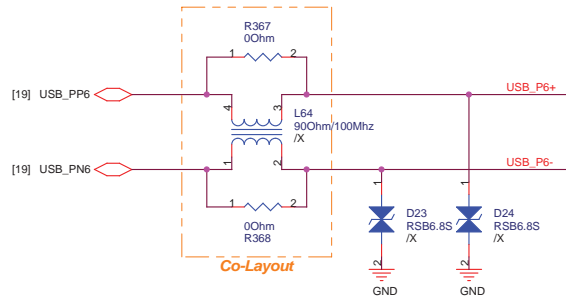


Normal type  
High: Slave  
Low :  
Master

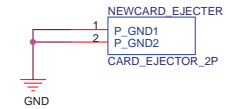




MINI CARD NUT(6.4mm) \*2

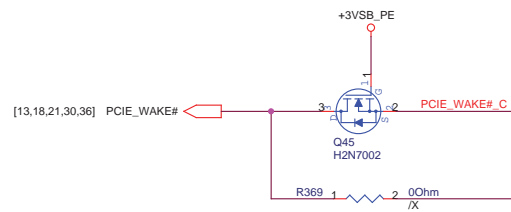
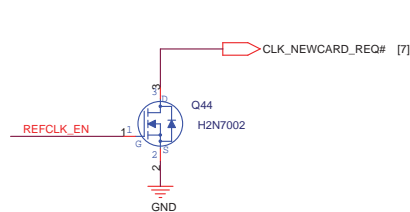
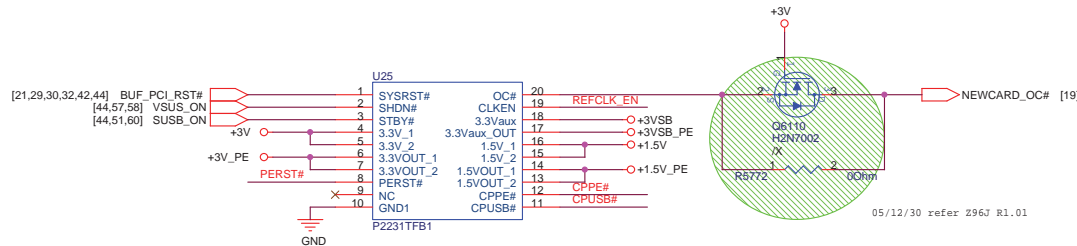
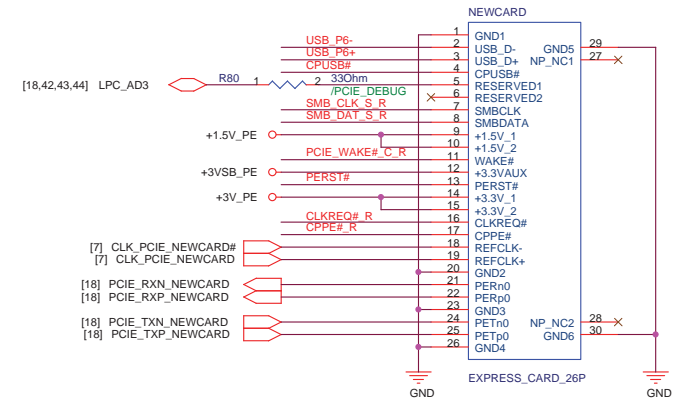


### NewCard Ejecter

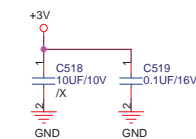


**!! ExpressCard Standard 1.0:**  
 Change Pin7 from RESERVED to SMBCLK  
 Change Pin8 from SMBCLK to SMBDATA  
 Change Pin9 from SMBDATA to +1.5V

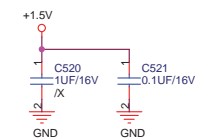
### NewCard Header



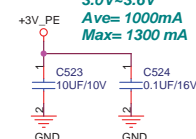
**3.0V-3.6V**  
 Ave= 200mA  
 Max= 275 mA



**3.0V-3.6V**  
 Ave= 1000mA  
 Max= 1300 mA



**1.35V-1.65V**  
 Ave= 500 mA  
 Max= 650 mA



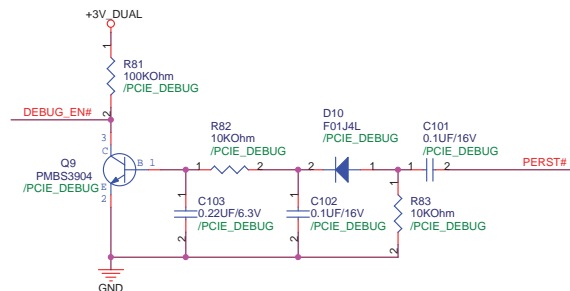
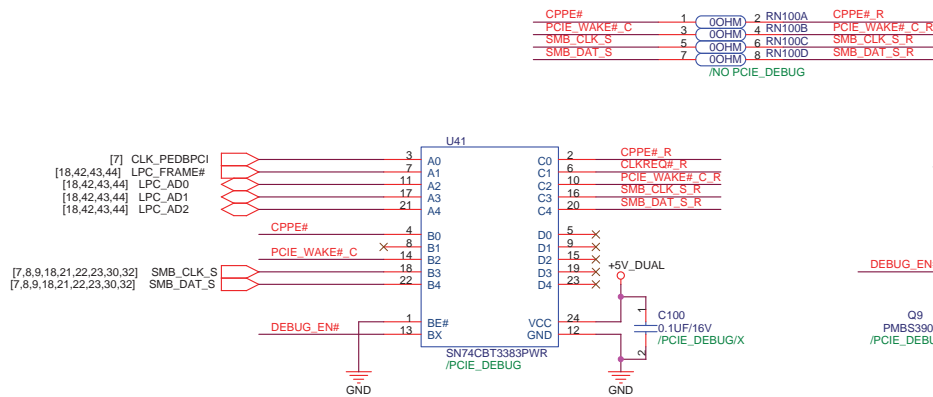
**3.0V-3.6V**  
 Ave= 200mA  
 Max= 275 mA

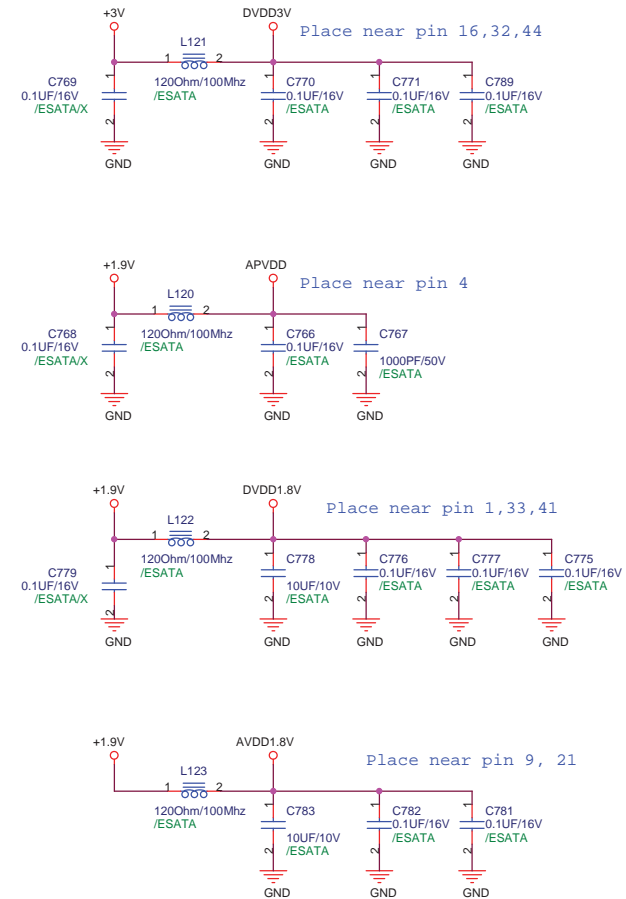


**3.0V-3.6V**  
 Ave= 1000mA  
 Max= 1300 mA

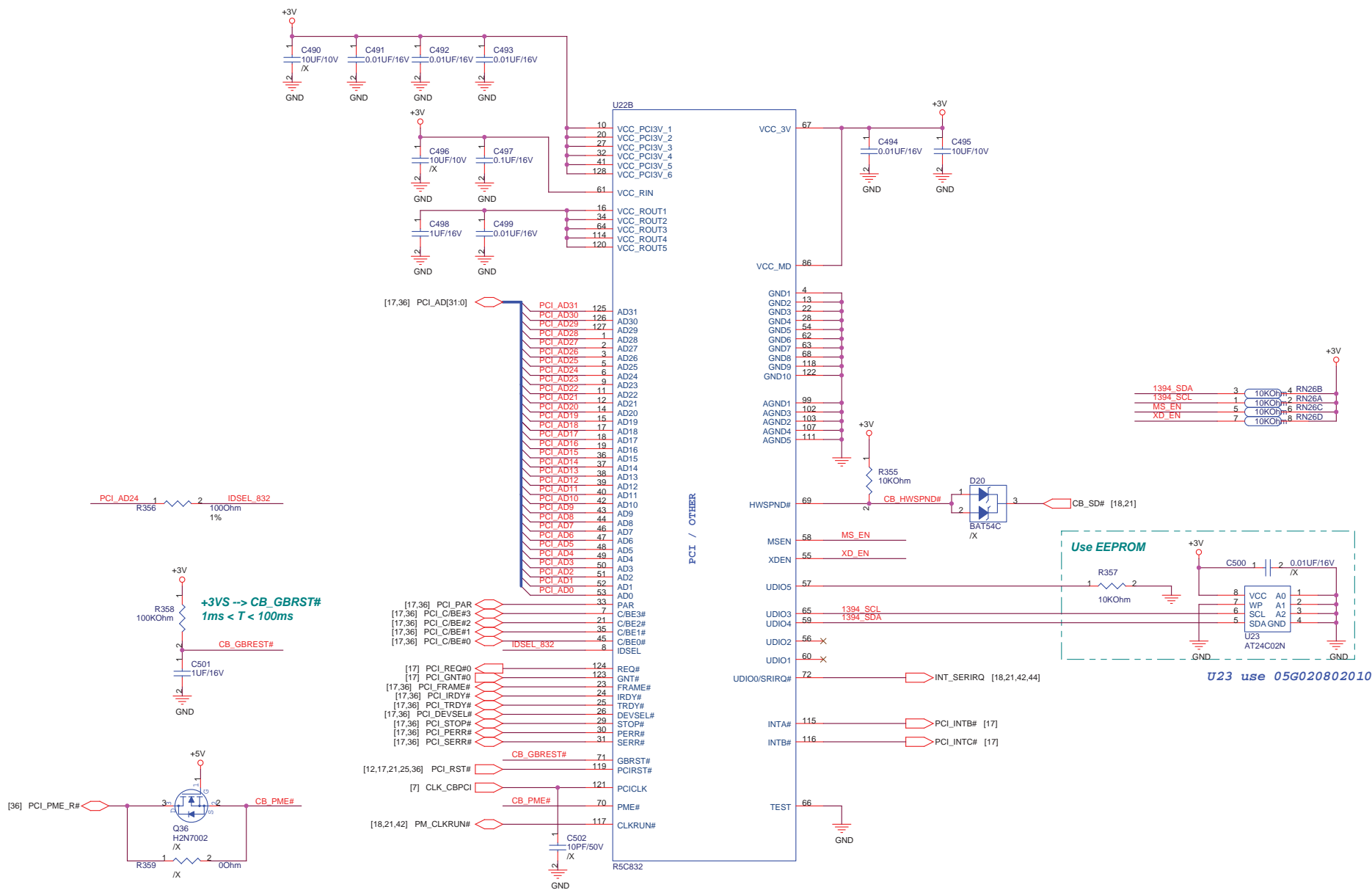


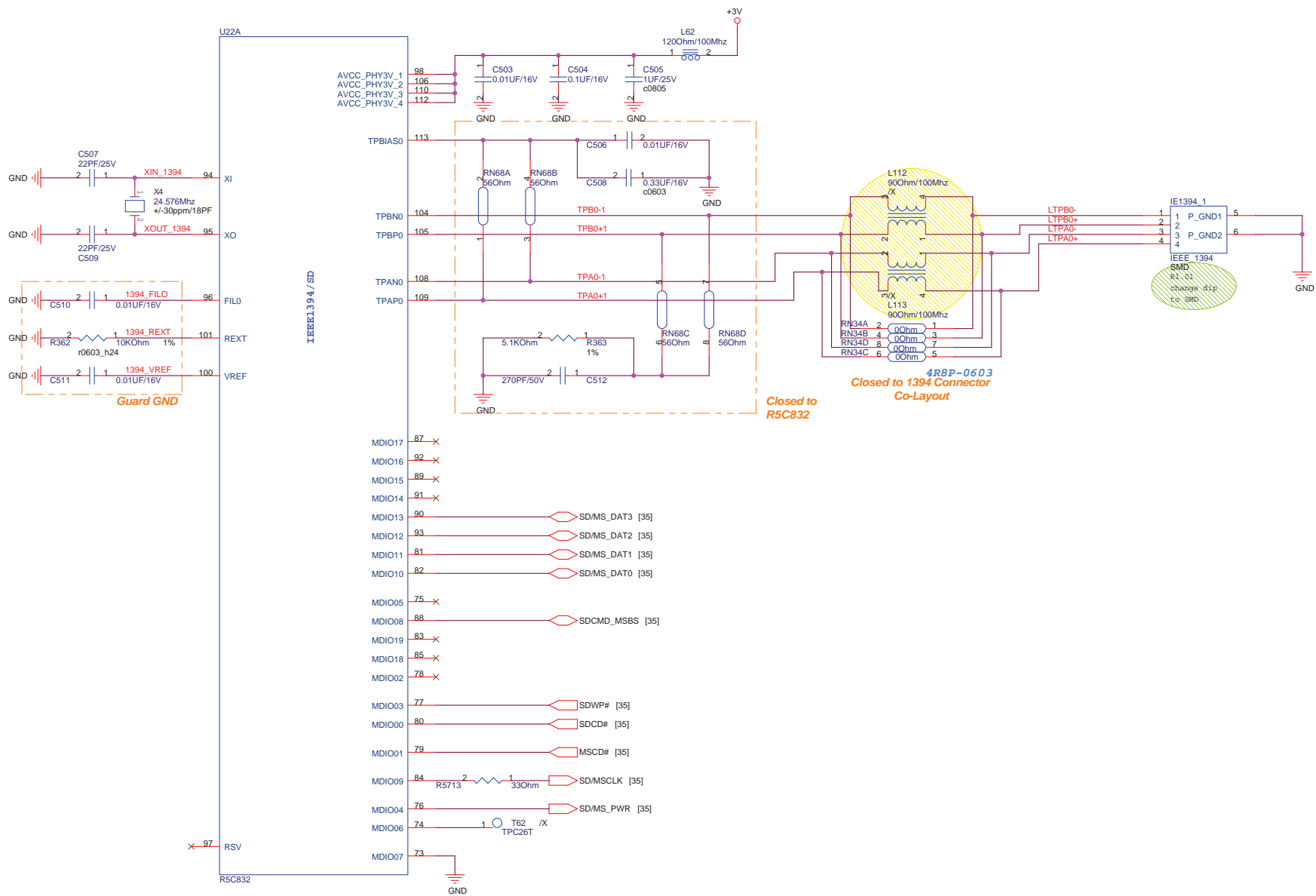
**1.35V-1.65V**  
 Ave= 500 mA  
 Max= 650 mA

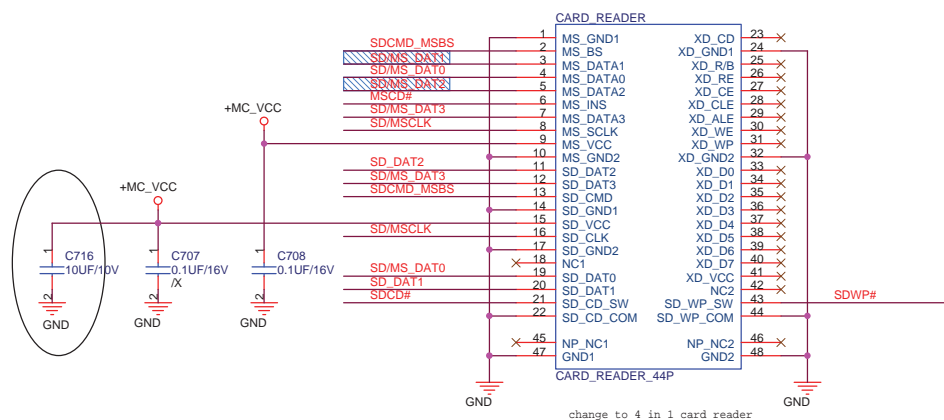
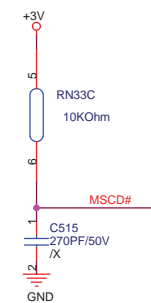
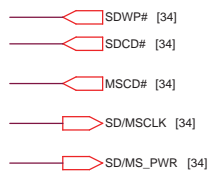


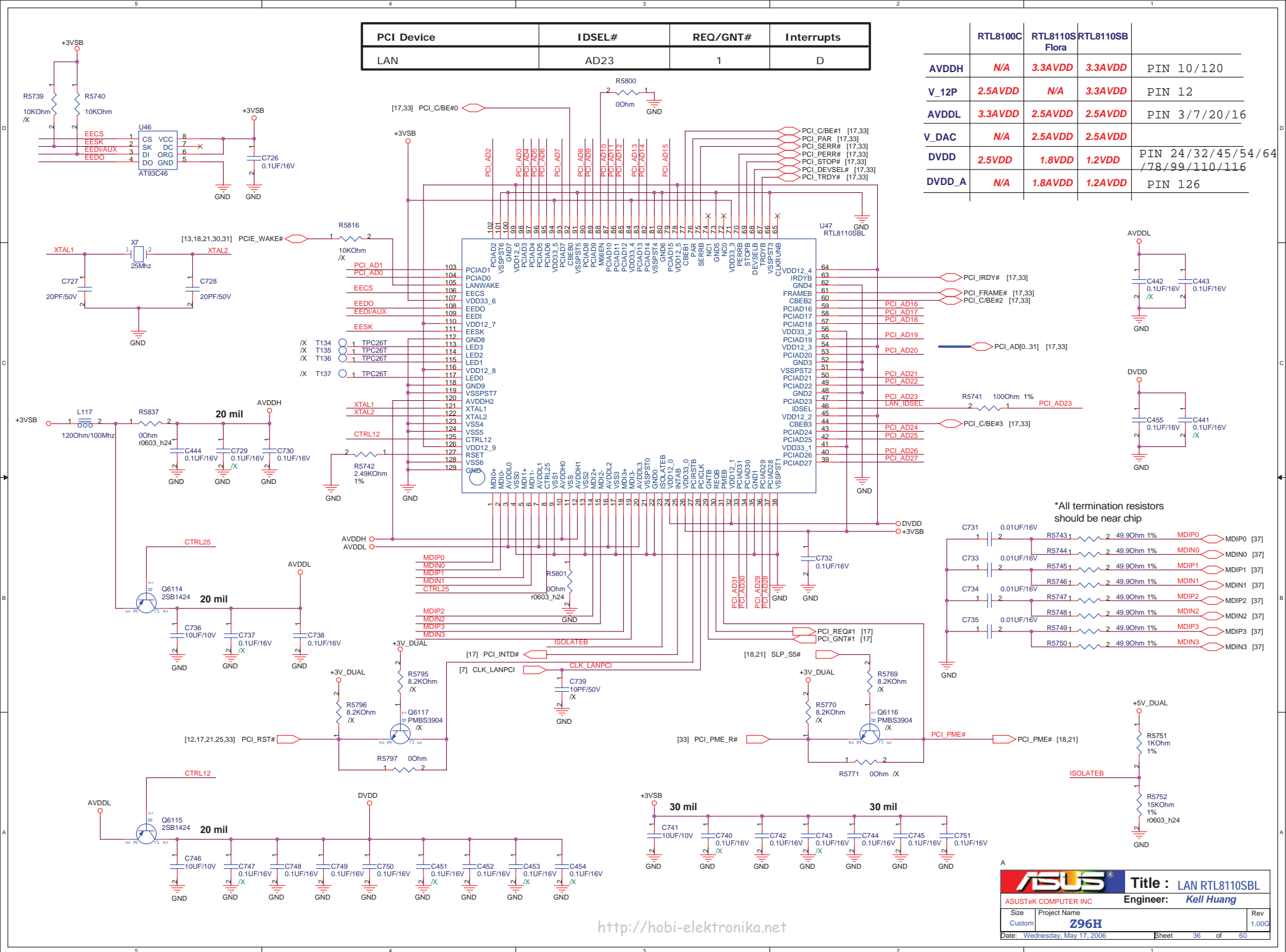




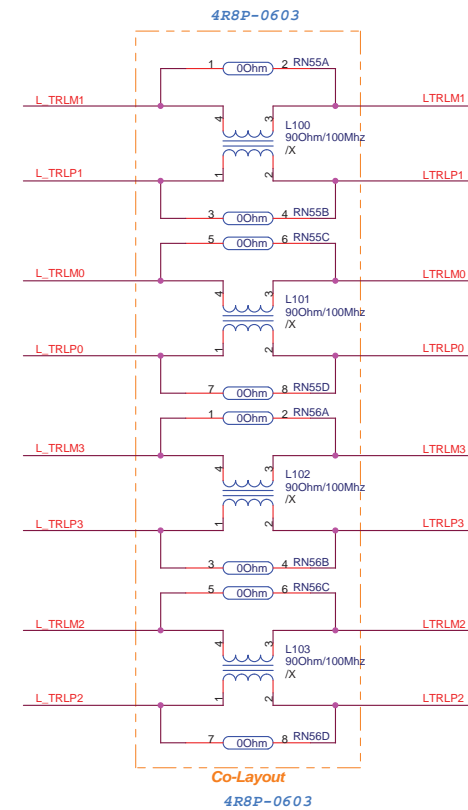
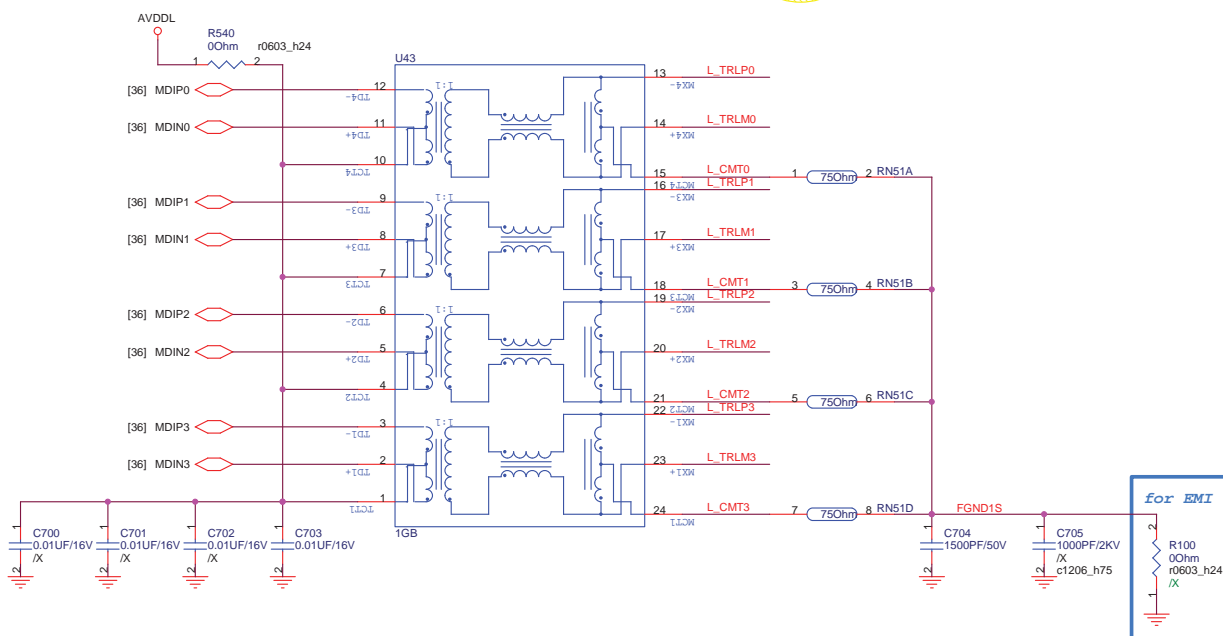
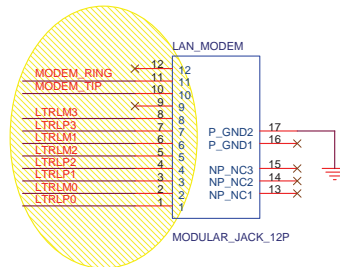
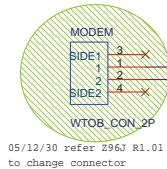
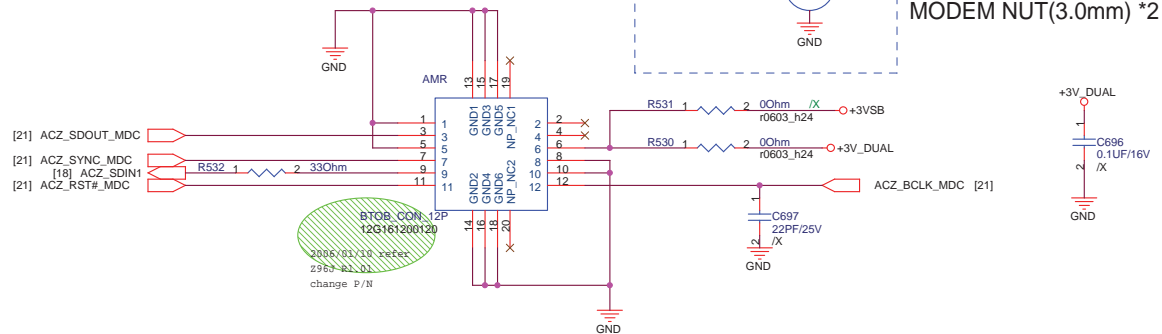


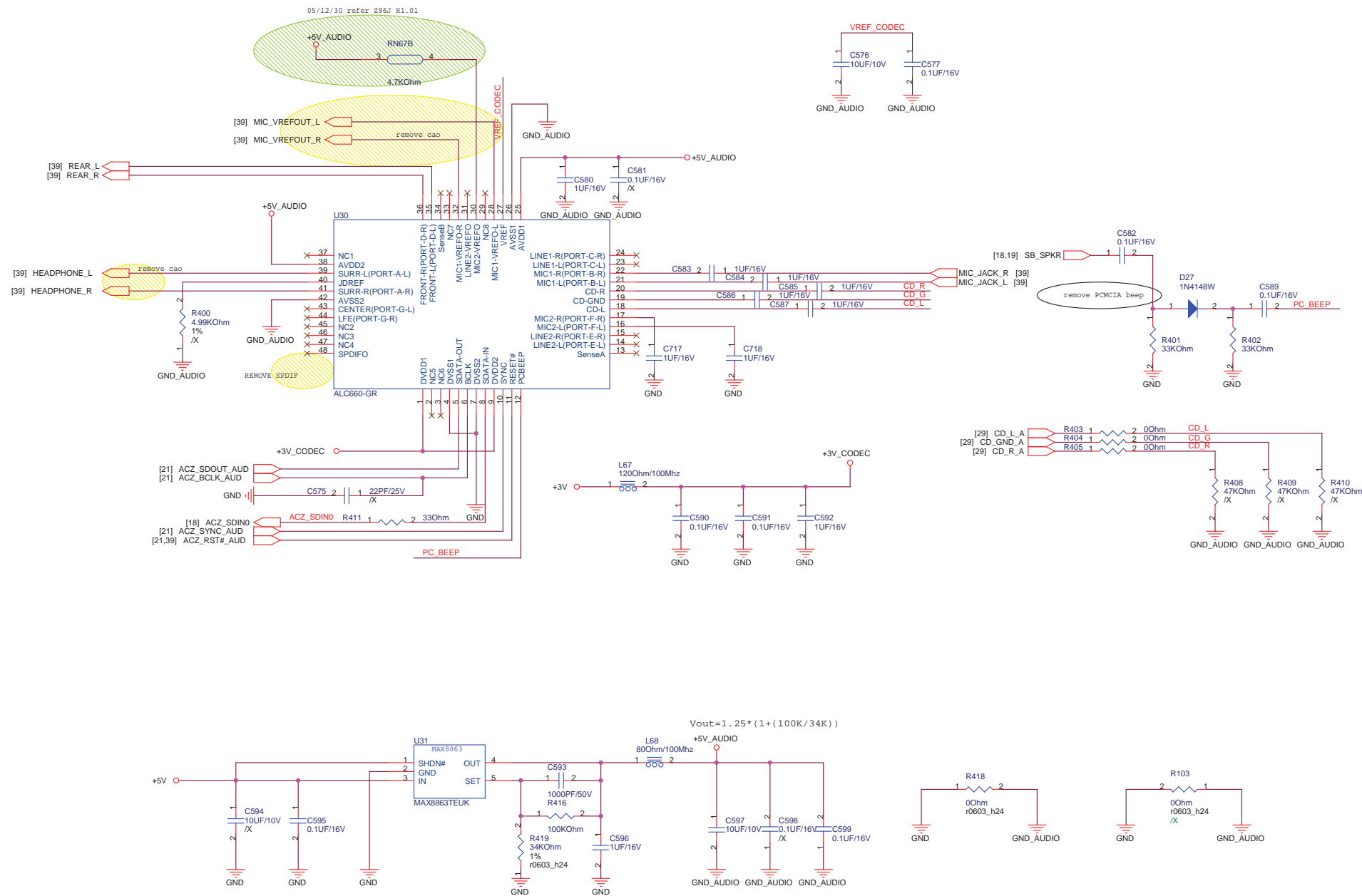


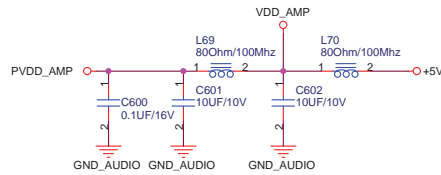
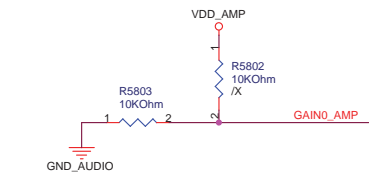




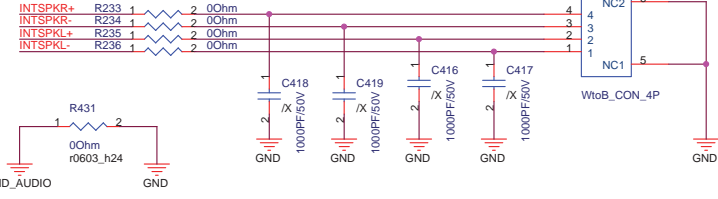
# MDC CONN.



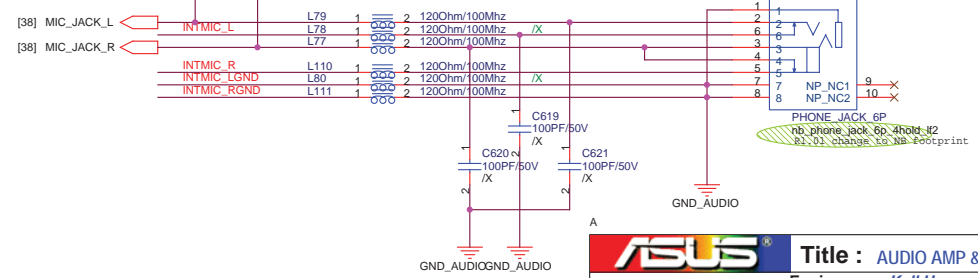
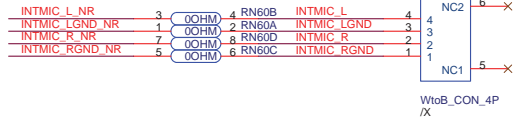
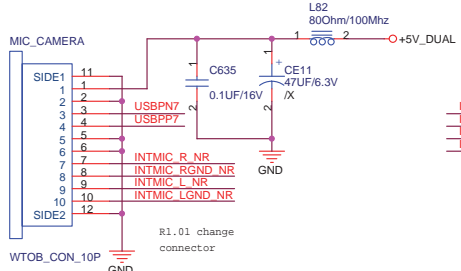
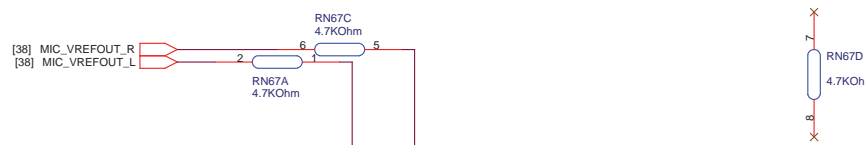
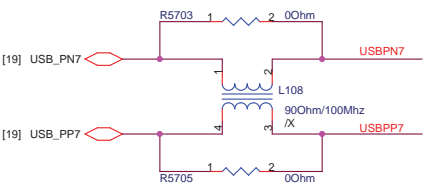
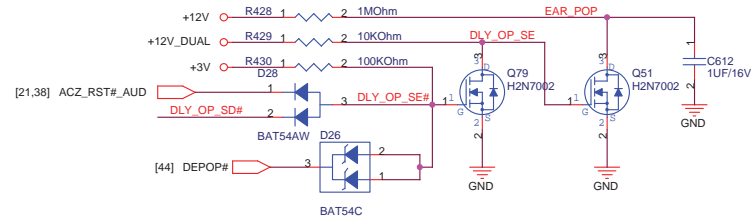
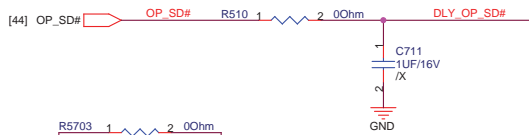
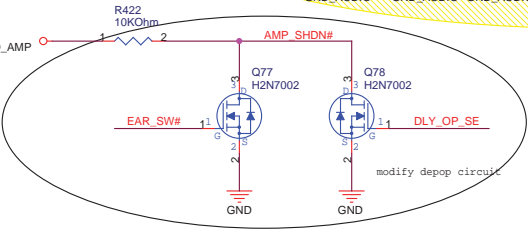
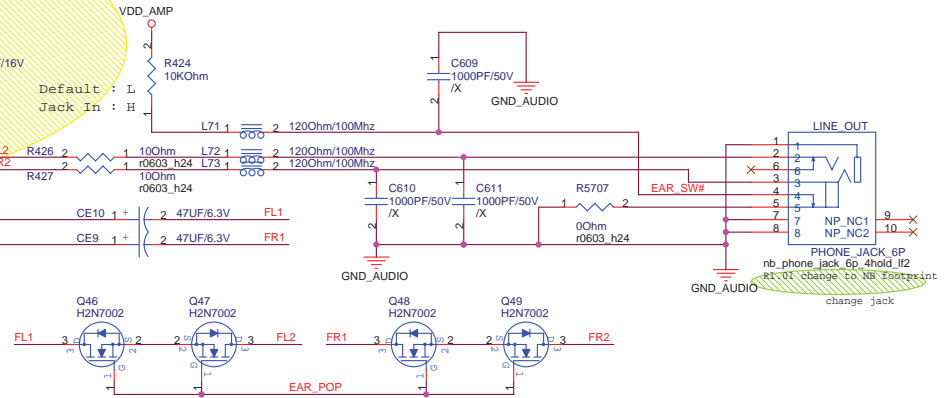
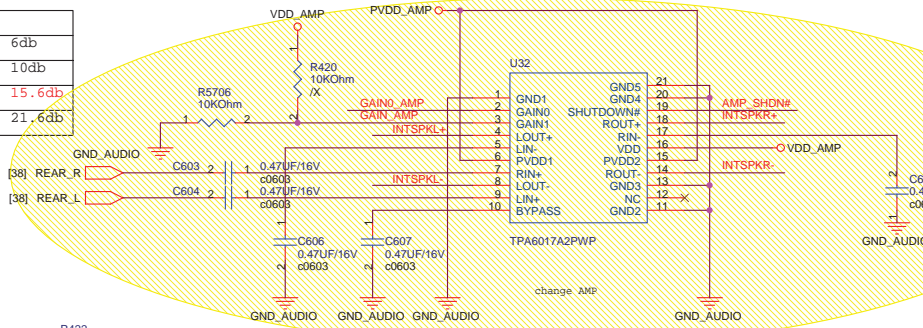




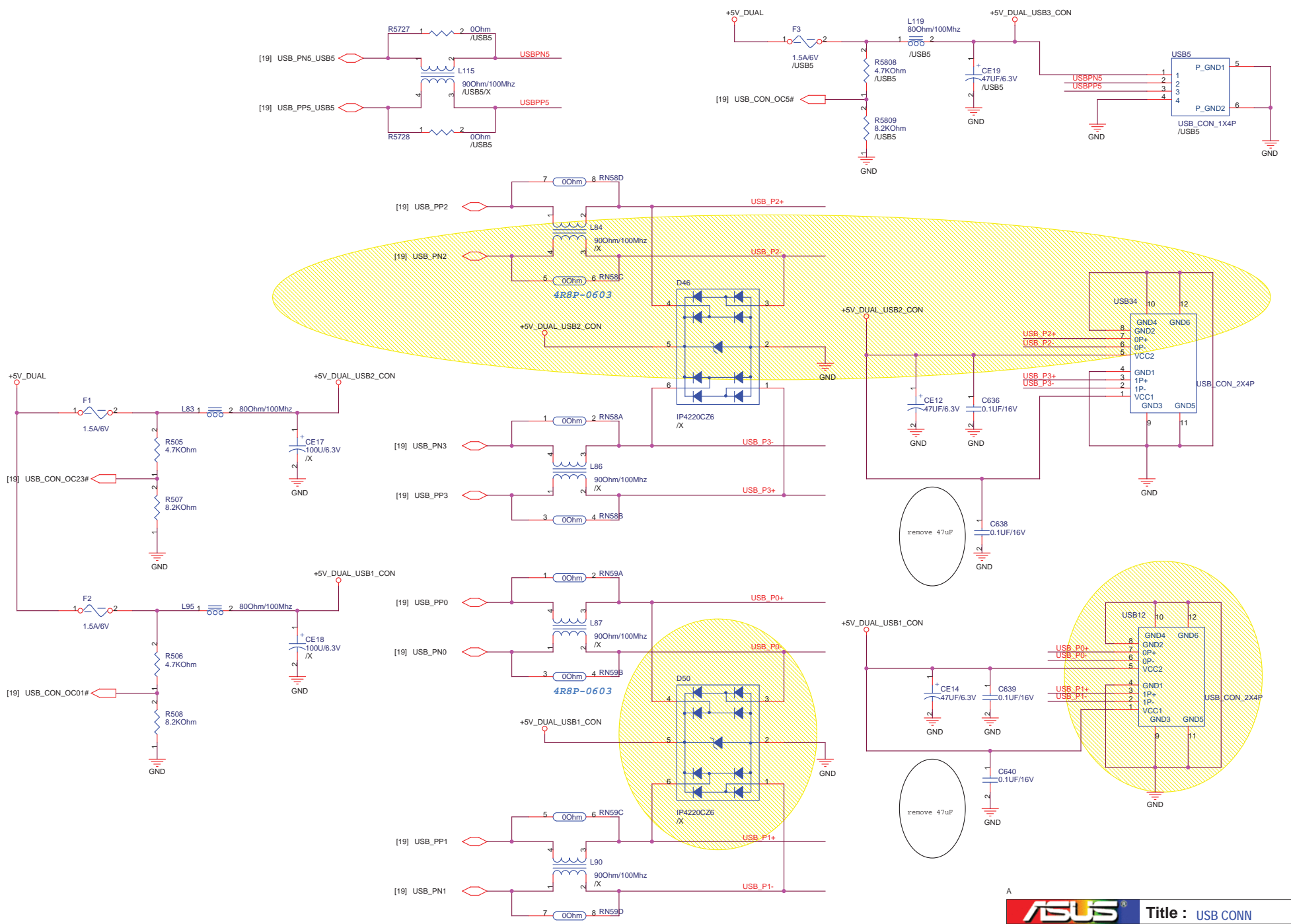
To Internal Speaker Connector



GAIN1	GAIN0	
0	0	6db
0	1	10db
1	0	15.6db
1	1	21.6db



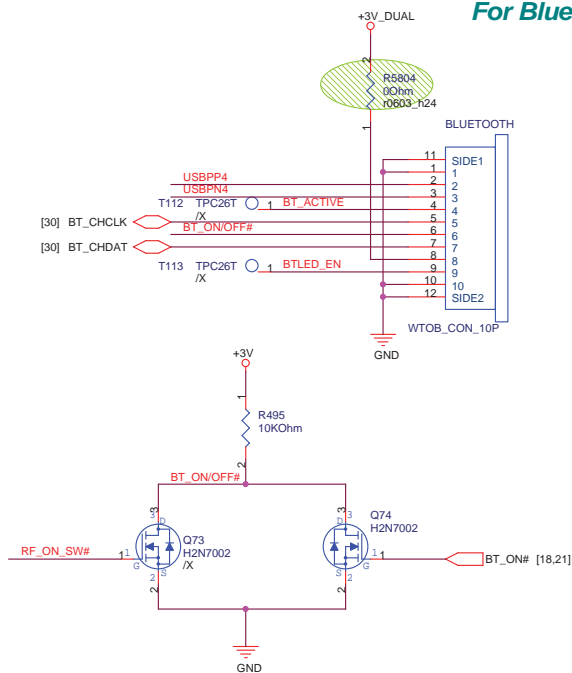
Microphone In Jack



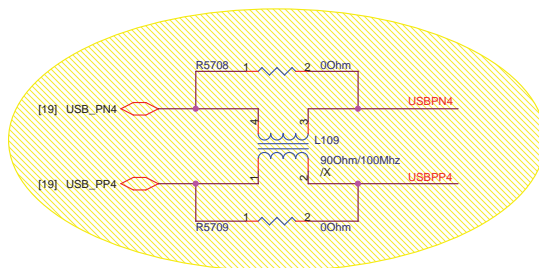
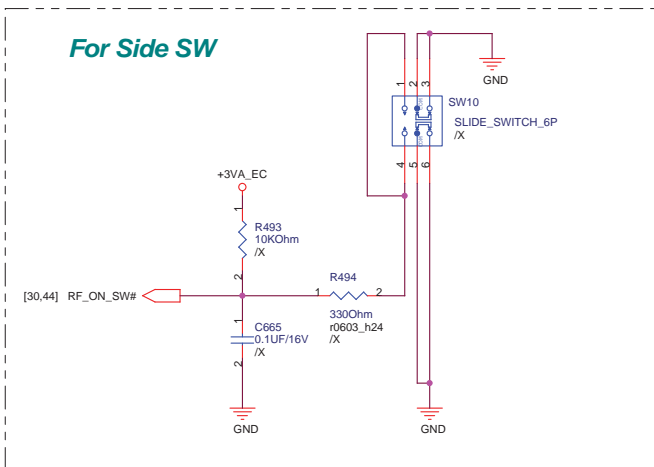
<http://hobi-elektronika.net>



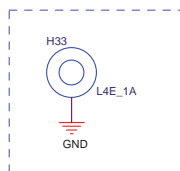
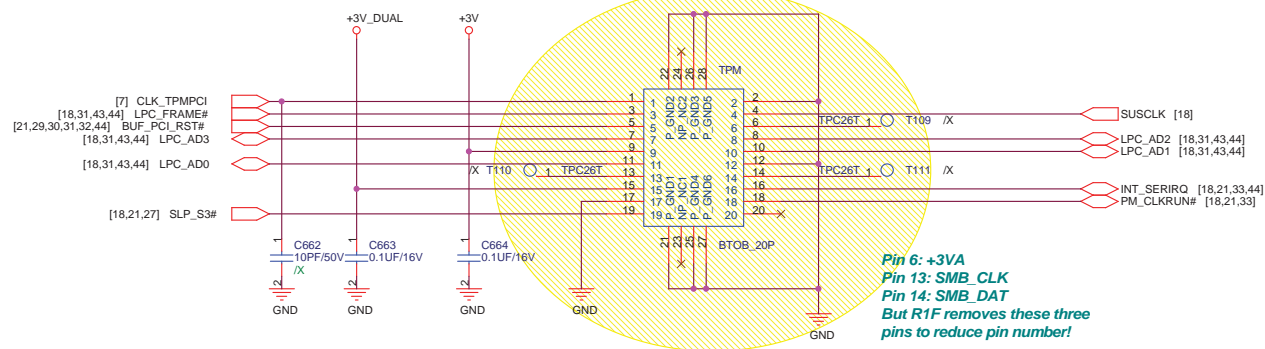
# For Bluetooth



# For Side SW

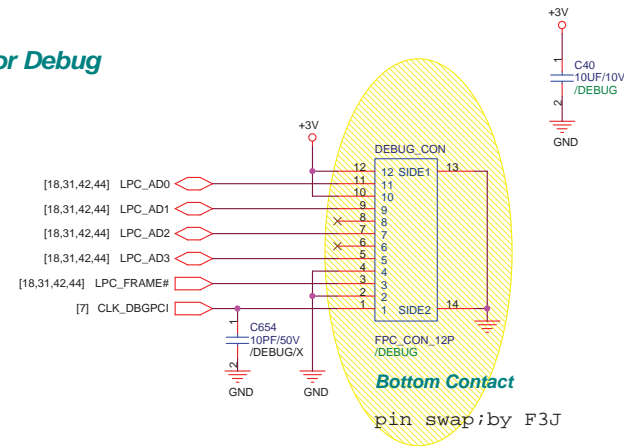


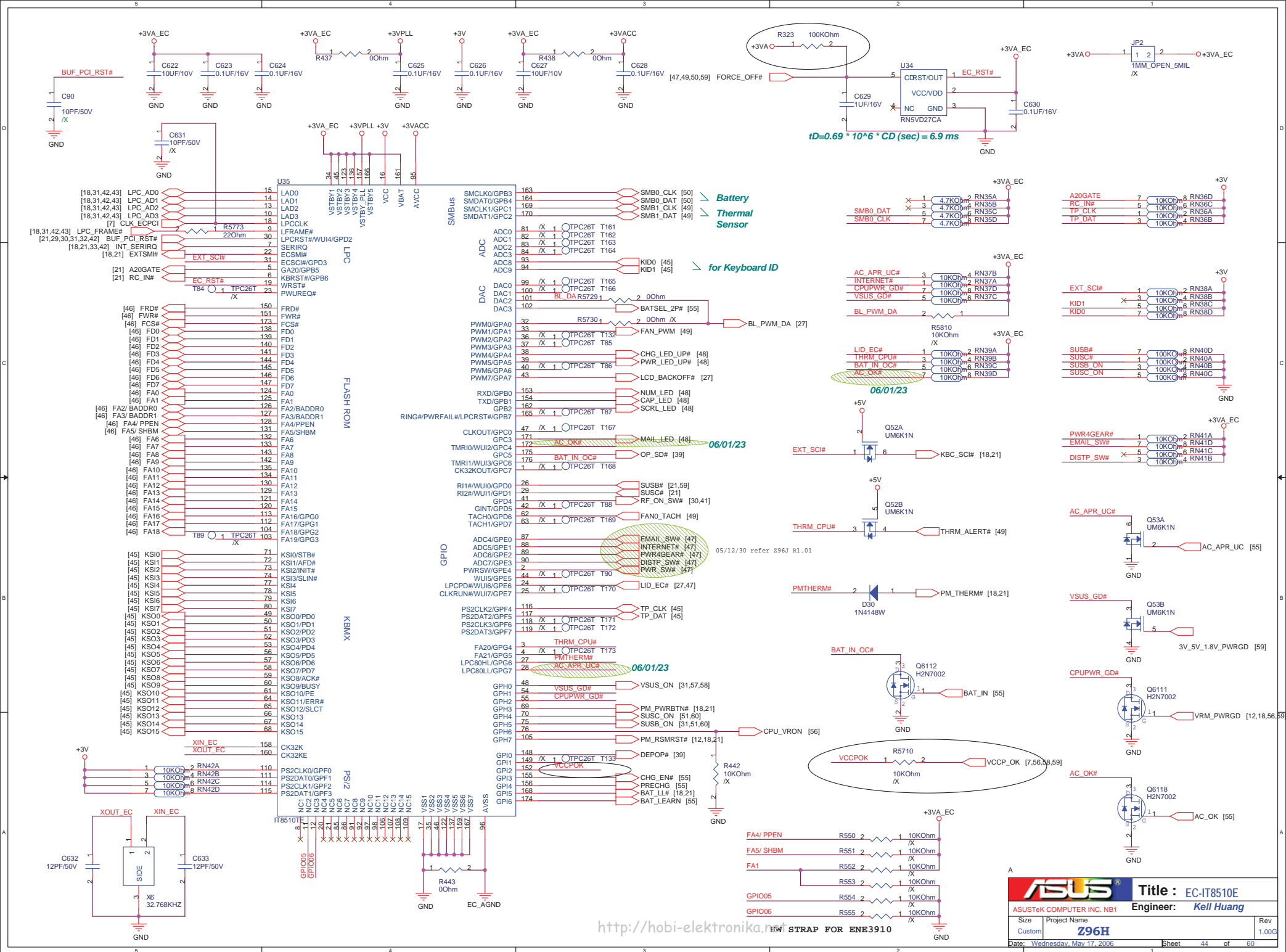
## For TPM Module



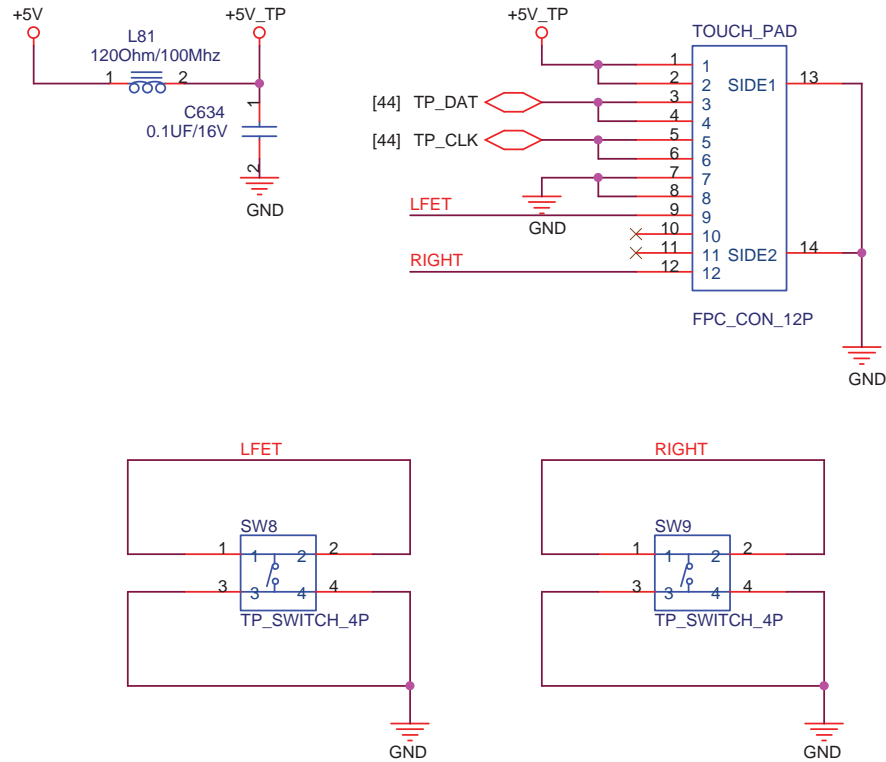
TPM MODULE NUT(3.0mm) \*1

*For Debug*

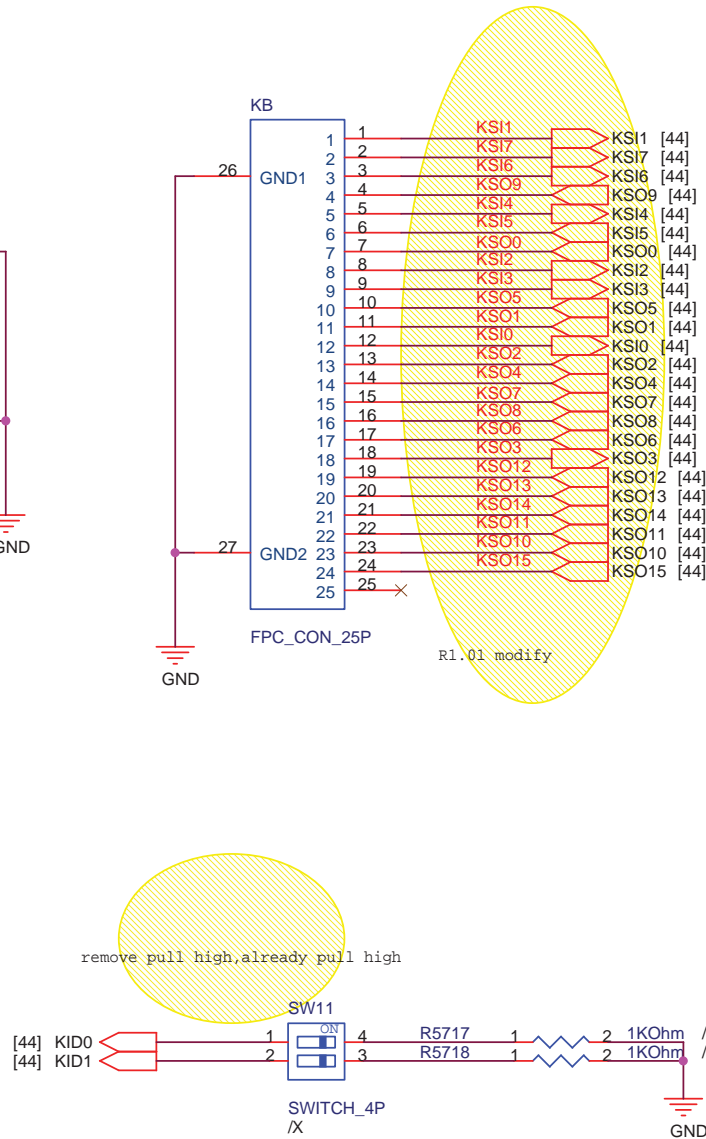




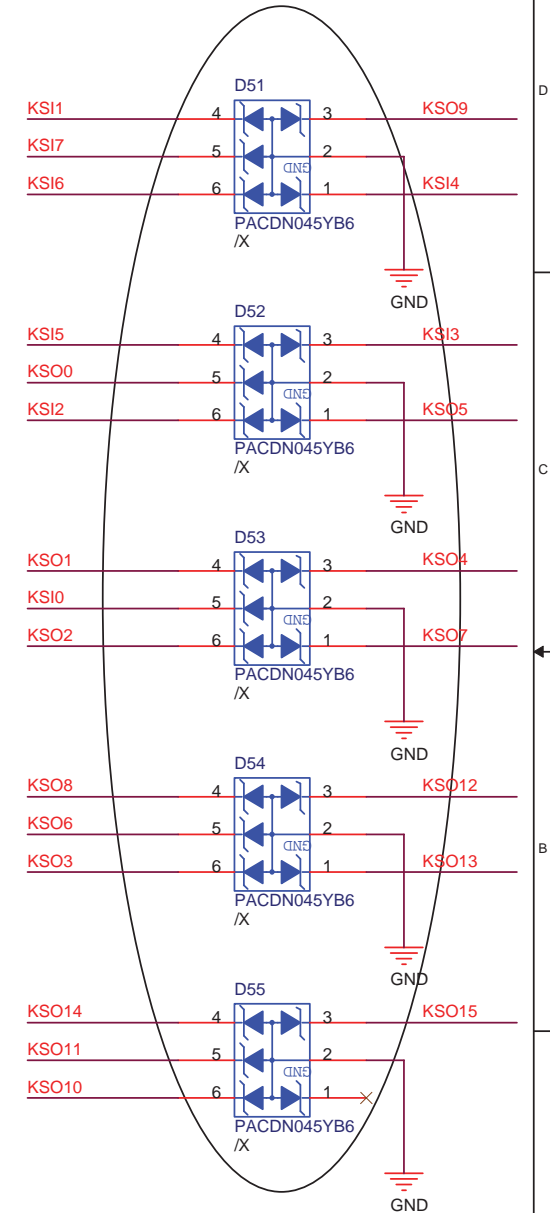
## For Touch-Pad



## For Keyboard



05/12/29 ESD DIODE PIN SWAPPED

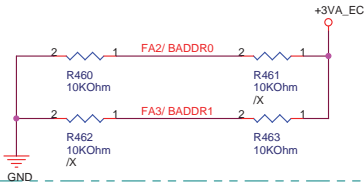


ISA ROM

EC Hardware Strapping

FA2/ BADDR0 & FA3/ BADDR1

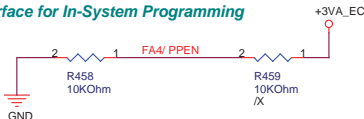
00: PNPCNG Access Register Pair Are 002Eh and 002Fh  
10: PNPCNG Access Register Pair Are 004Eh and 004Fh  
01: PNPCNG Access Register Pair Are Determined by EC Domain Registers SWCBALR and SWCBAHR.  
11: Reserved



Note: Sampled at VSTBY Power Up Reset

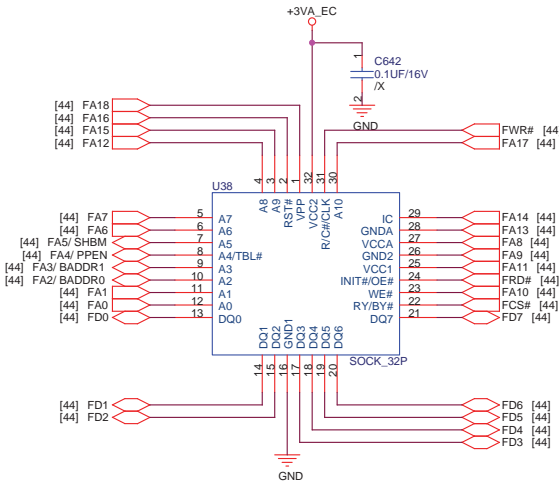
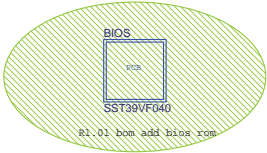
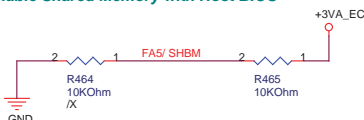
FA4/ PPEN

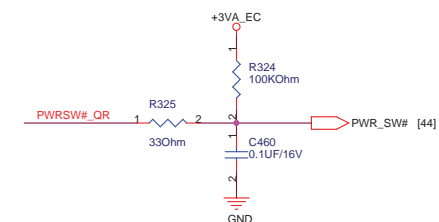
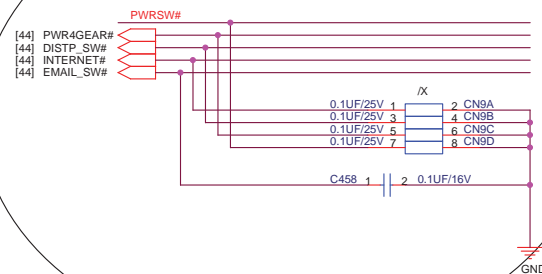
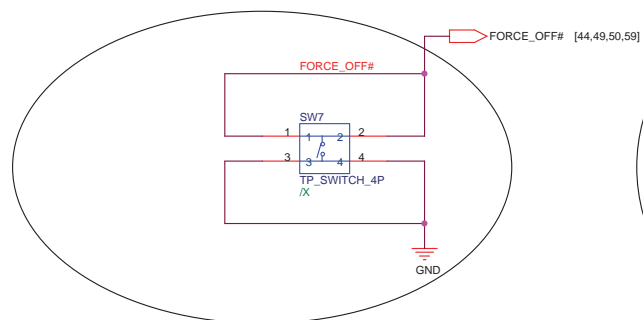
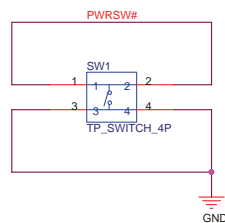
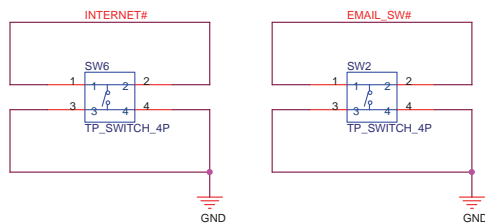
0: Normal  
1: KBS Interface Pins Are Switched to Parallel Port Interface for In-System Programming



FA5/ SHBM

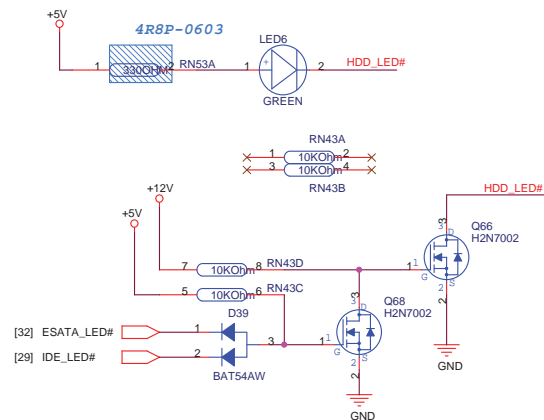
0: Disable Shared Memory with Host BIOS  
1: Enable Shared Memory with Host BIOS



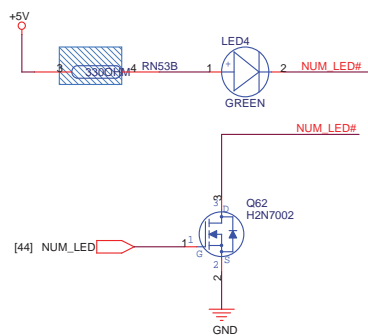


**For LED**

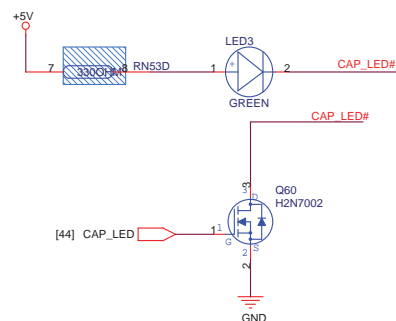
**For SATA/IDE LED**



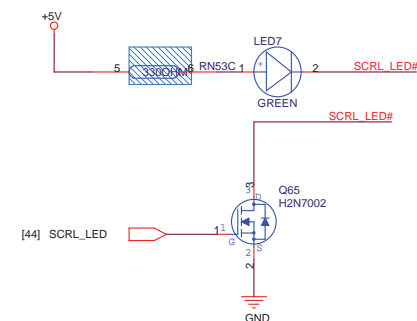
**for Num Lock**



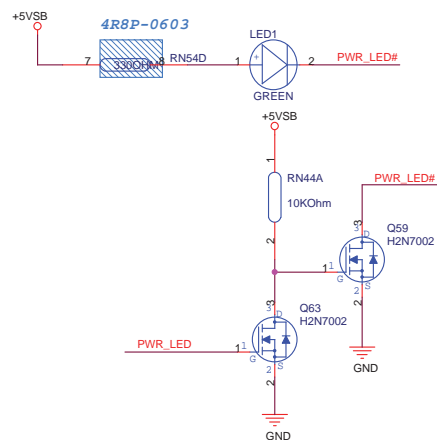
**for Cap. Lock**



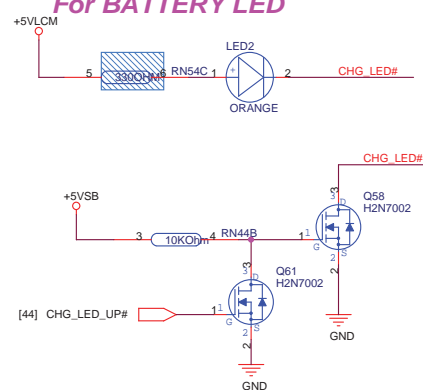
### for Scroll Lock



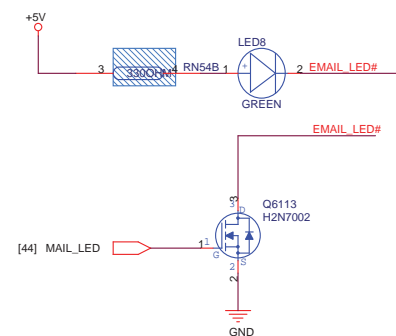
**For POWER LED**



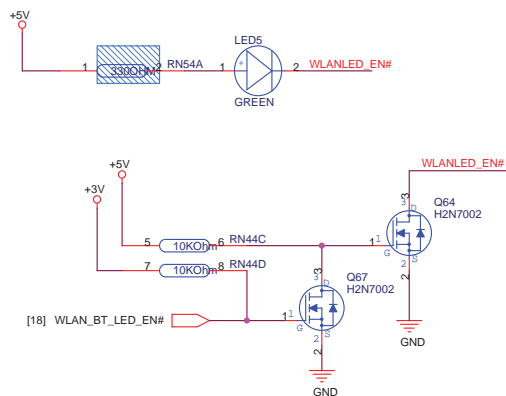
**For BATTERY LED**



**for email**

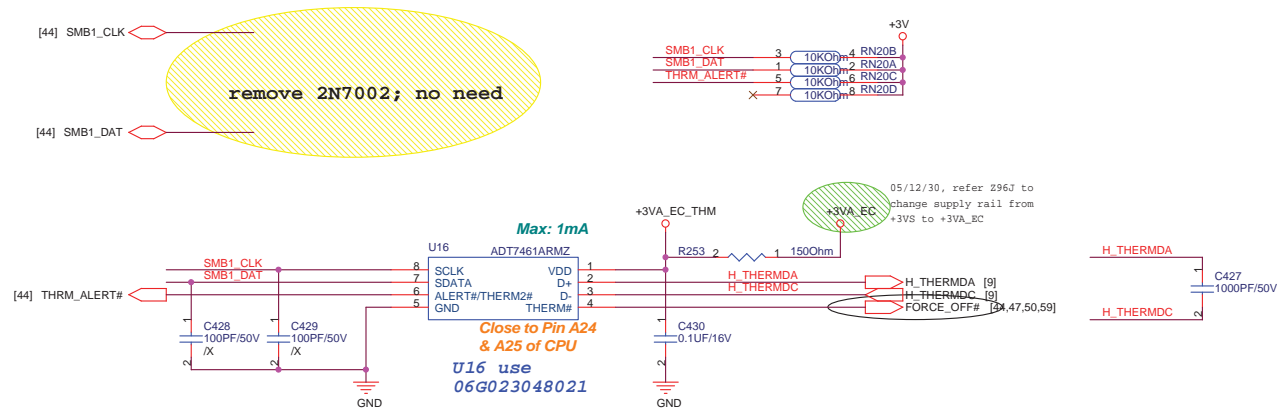


**For WireLess LED**





## Thermal Sensor



Route H\_THERMDA and H\_THERMDC on the same layer

OTHER SIGNALS

15 mils

GND

10 mils

H\_THERMDA(10 mils)

10 mils

H\_THERMDC(10 mils)

10 mils

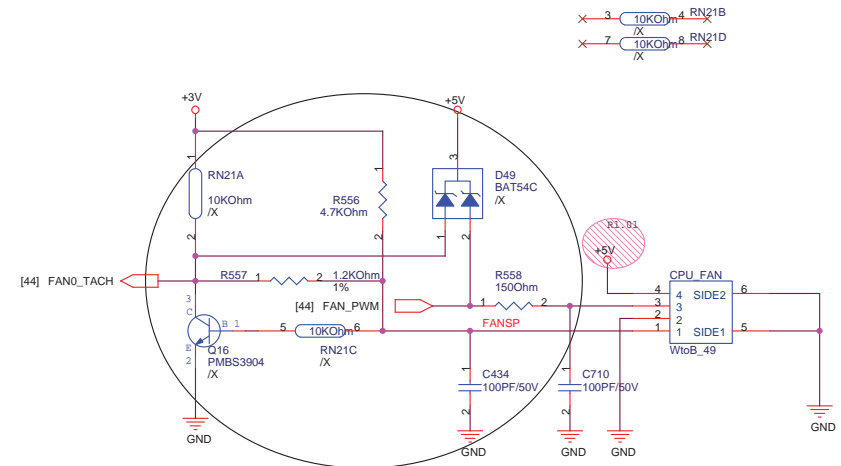
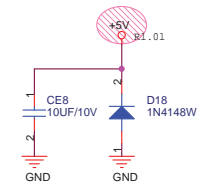
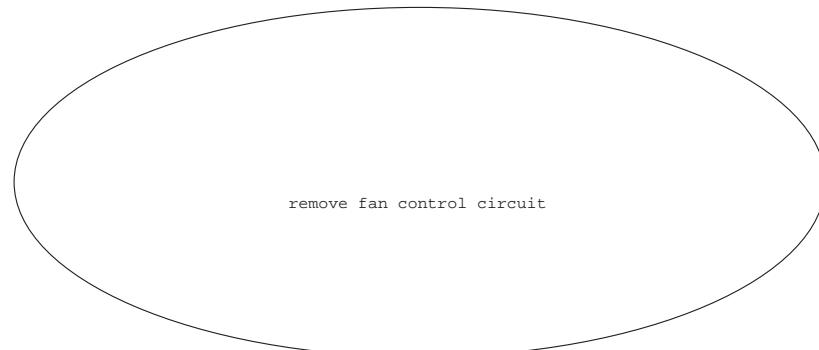
GND

15 mils

OTHER SIGNALS

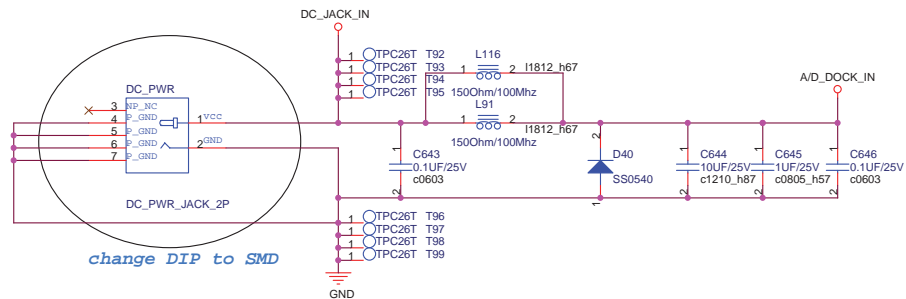
Avoid FSB,Power

## DC FAN Control



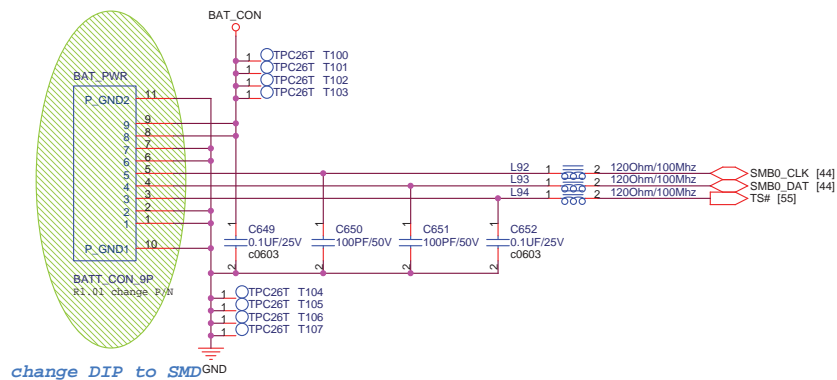
CPU FAN will be forced on:  
1) Thermal Sensor Over-temperature  
2) WATCHDOG asserted by EC

## DC IN

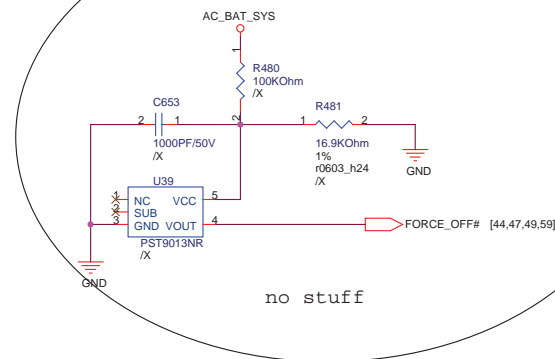


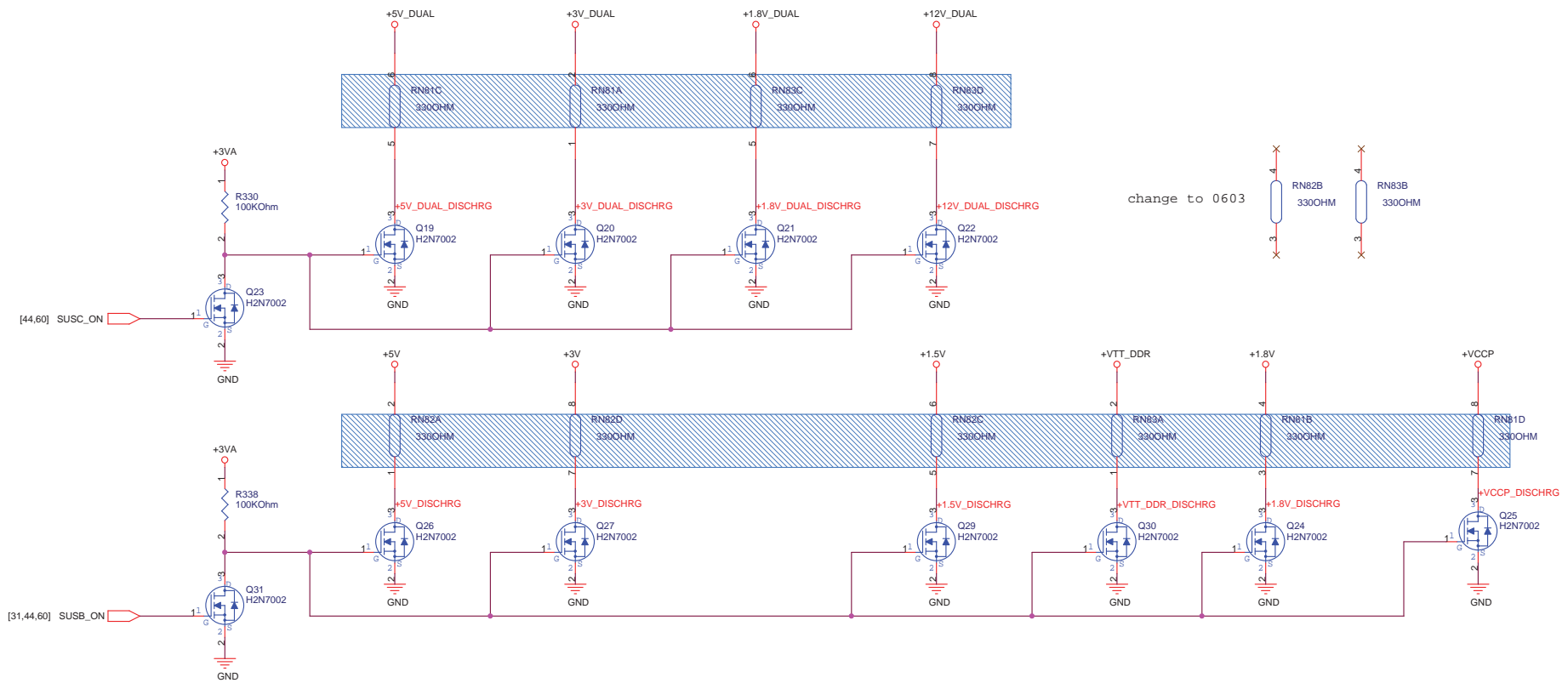
remove AC DC detect; no need

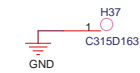
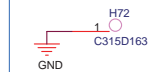
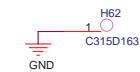
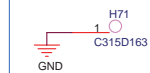
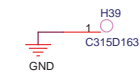
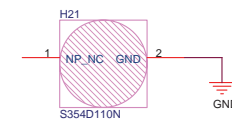
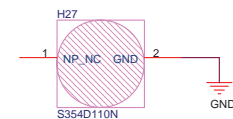
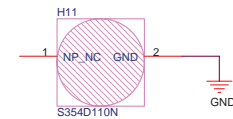
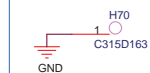
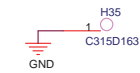
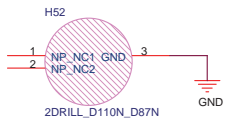
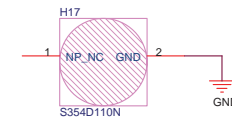
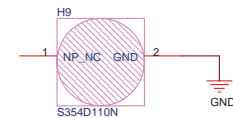
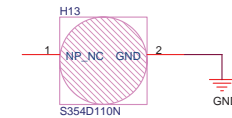
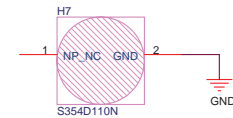
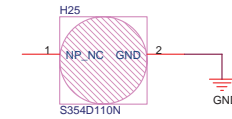
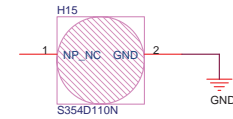
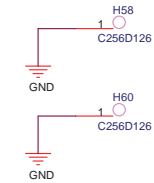
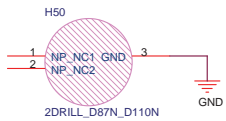
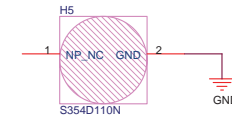
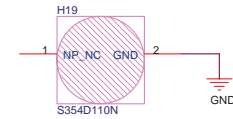
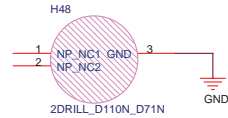
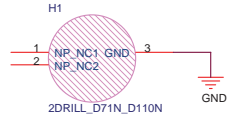
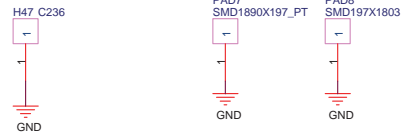
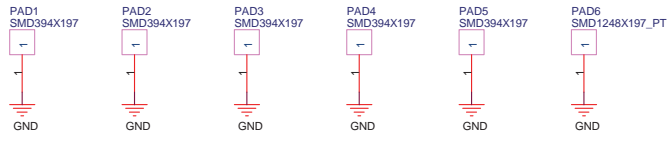
## BAT IN



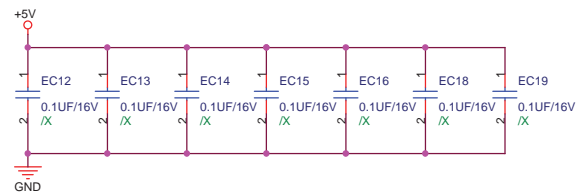
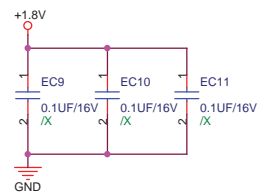
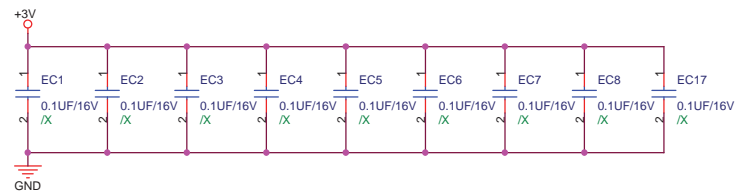
## Without Battery & Pull out Adapter

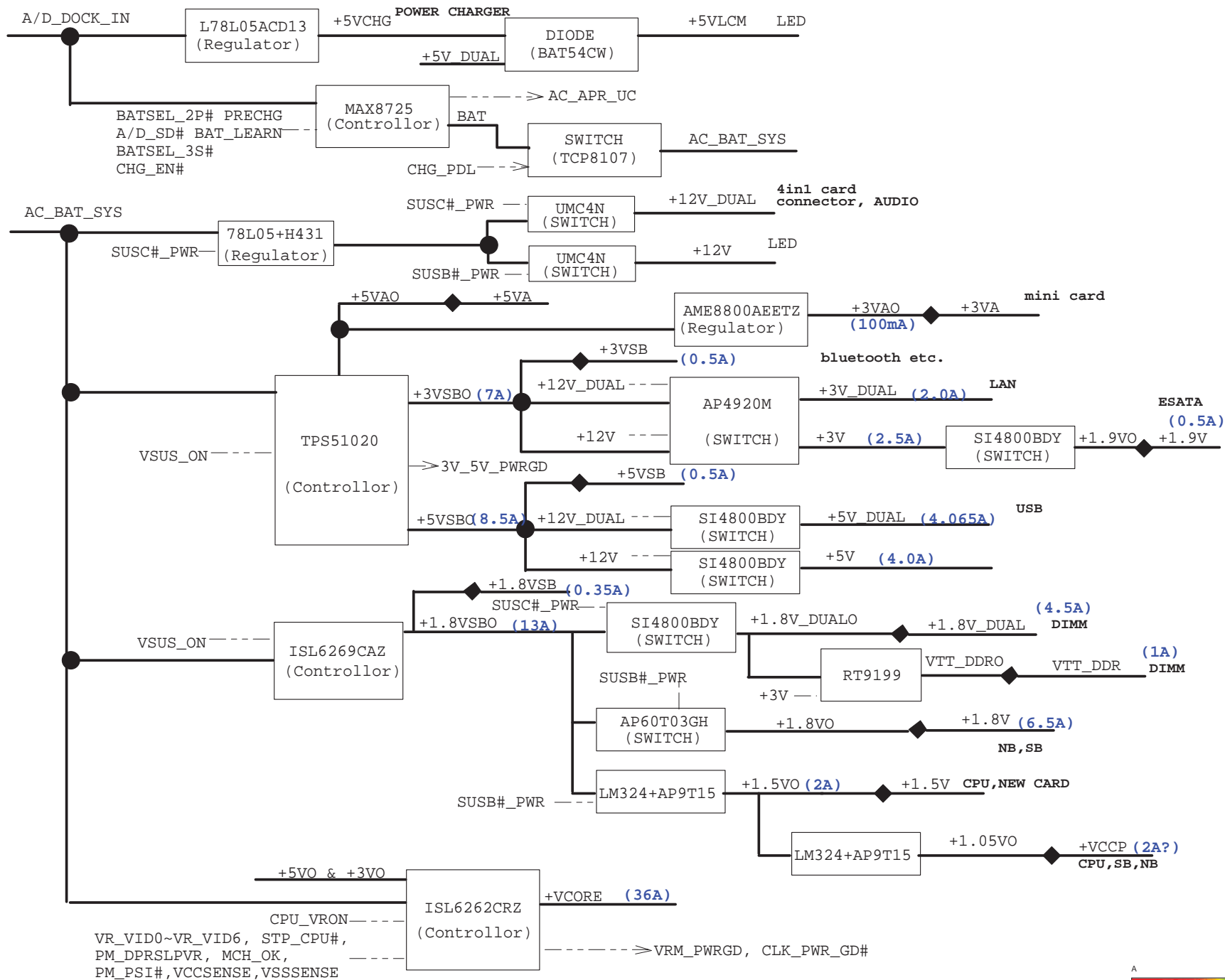






for NB





## POWER PATH & BAT\_LEARN

AC\_IN Threshold 2.048Vmax A/D\_DOCK\_IN

> 17.44V active

Adapter In(max) =  $[0.075V/Rsense(ADin)] \cdot [VCLSVREF]$   
 $Rsense(ADin) = 0.02 \text{ ohm}$   
 $VCLSV = 3.685V$   
 $\Rightarrow \text{In(max)} = 3.27A$   
 $\Rightarrow \text{Constant Power} = 19 \cdot 3.27 = 62.13W$   
 $\Rightarrow R5710 = 20K, R5715 = 137K$

Adapter In(max) =  $[0.075V/Rsense(ADin)] \cdot [VCLSVREF]$   
 $VCLSV = 2.885V$   
 $\Rightarrow \text{In(max)} = 2.544A$   
 $\Rightarrow \text{Constant Power} = 19 \cdot 2.44 = 48.336W$   
 $\Rightarrow R5710 = 20K, R5715 = 42.2K$

Charge Current  $I_{chg} = [0.075V/Rsense(CHG)] \cdot [VICTL/3.6V]$   
 $Rsense(CHG) = 25m \text{ Ohm}$   
 $VICTL = 3V \Rightarrow I_{chg} = 2.5A$   
 $VICTL = 1.68V \Rightarrow I_{chg} = 1.4A$

$V_{bat} = \text{Cell} \cdot [Vref + ((VICTL - 1.8V) / 9.52)]$   
 $VICTL = 1.585V$   
 $\Rightarrow V_{bat} = 4.2V$

VICTL < 0.8V or DCIN < 7V → Charger Disable

MODE (Pin7)	Battery
High (>2.8V)	4-Cell
Low (<0.8V)	3-Cell
High Impedance (1.6V < Vmode < 2V)	Battery Learn

MAX8725\_REF : 4.2235V  
 MAX8725\_LDO : 5.4V

### Battery Charging Voltage :

$+V_{BAT} = 4 \times [4.2235 + (V_{ictl} - 1.8) / 9.52]$

### Battery Charging Current :

$I_{charge} = (0.075 / PR5706) \times (V_{ictl} / 3.6)$

### Input Adaptor Max. Current Limit :

$I_{limit\_current} = (0.075 / PR5701) \times (V_{cls} / 4.2235)$

### Pre-Charging Mode :

Precharging current = 163.9mA

$V_{ictl} = 0.098V$

### Battery Cell Selection :

BATSEL\_2P# = 1, 6 Cells;  $V_{ictl} = 1.678V$

$\Rightarrow I_{charge} = 2.331A$

BATSEL\_2P# = 0, 9 Cells;  $V_{ictl} = 2.785V$

$\Rightarrow I_{charge} = 3.868A$

CHG\_EN# = 1, Charger Disabled  
 CHG\_EN# = 0, Charger Enabled

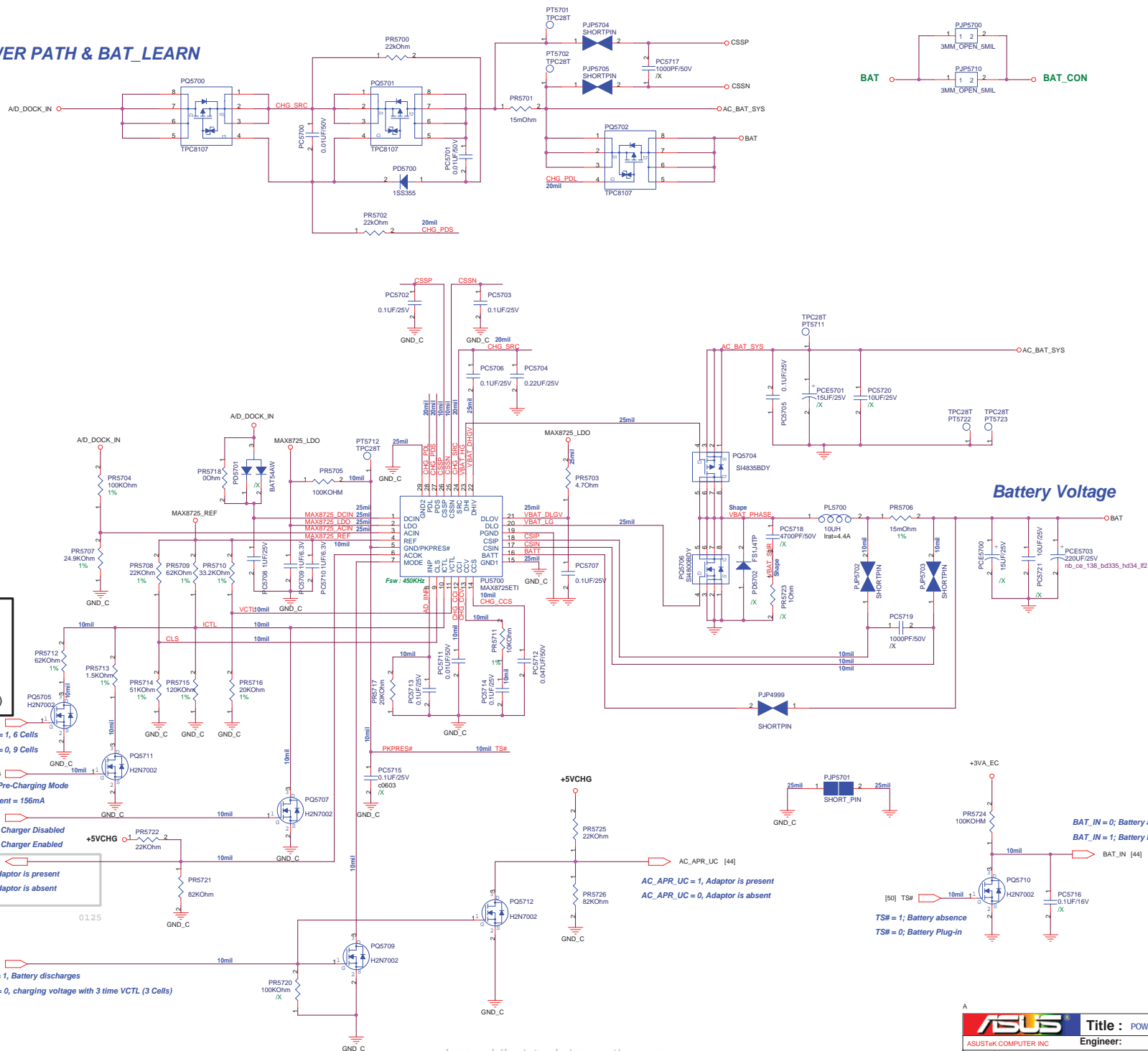
AC\_OK  
 AC\_OK = 1, Adaptor is present  
 AC\_OK = 0, Adaptor is absent

A/D\_SD# = 1. Enable charger

A/D\_SD# = 0. Disable charger

BAT\_LEARN  
 BAT\_LEARN = 1, Battery discharges

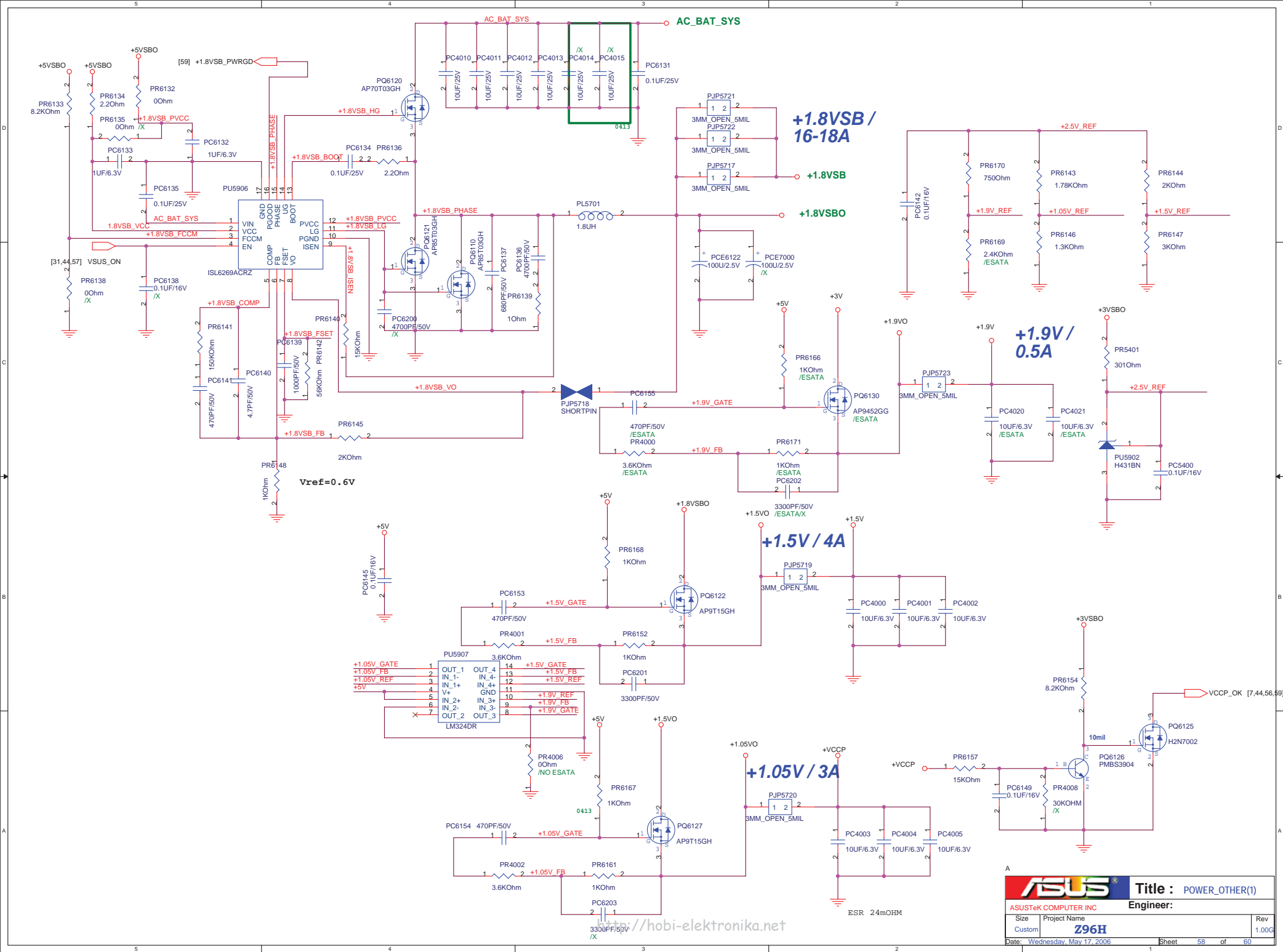
BAT\_LEARN = 0, charging voltage with 3 time VICTL (3 Cells)

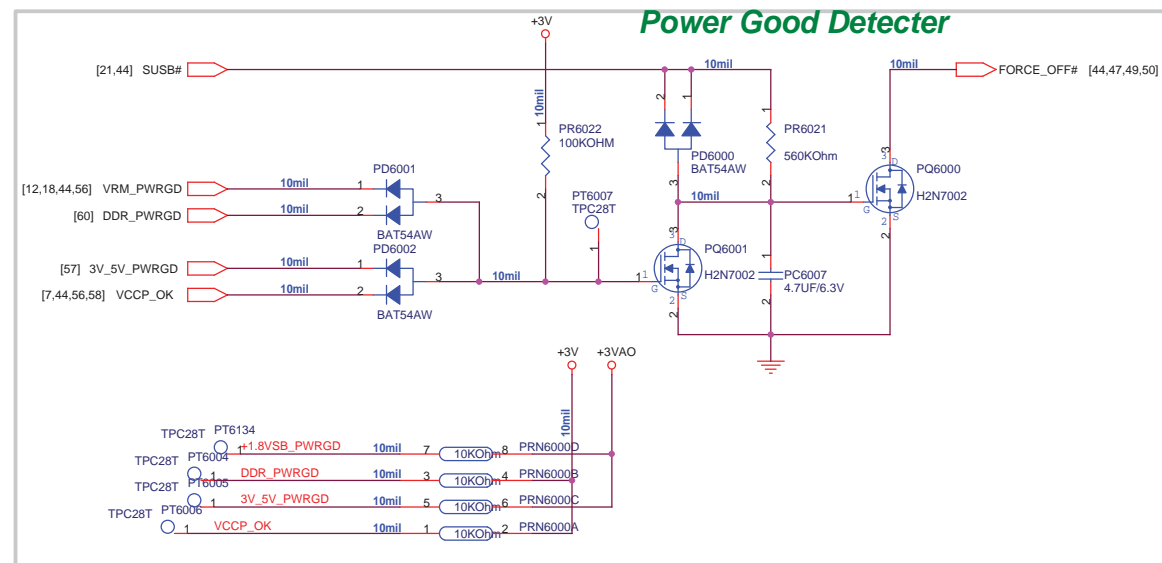
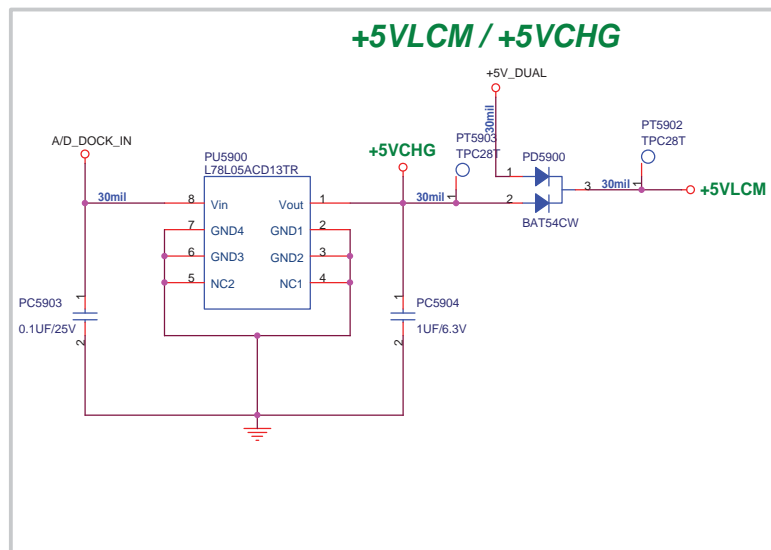
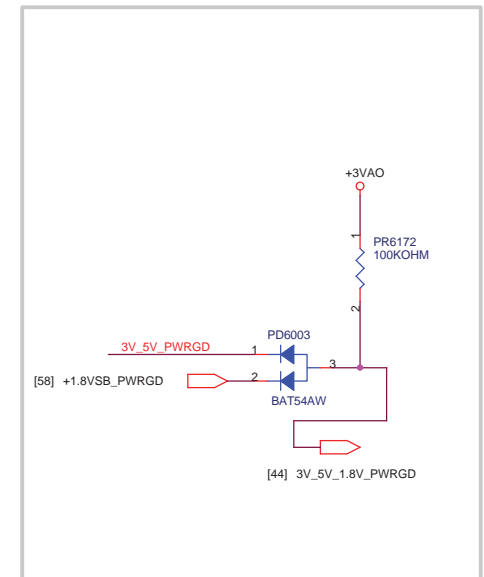
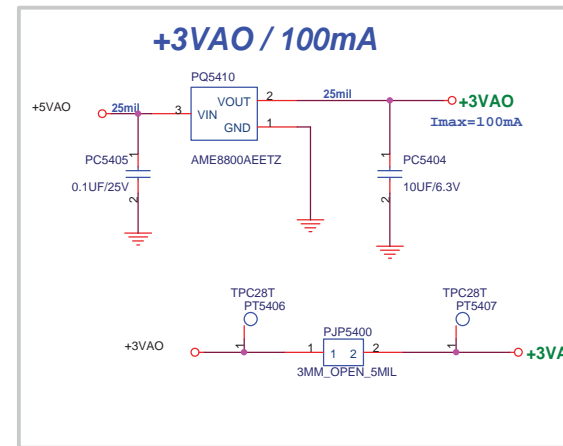
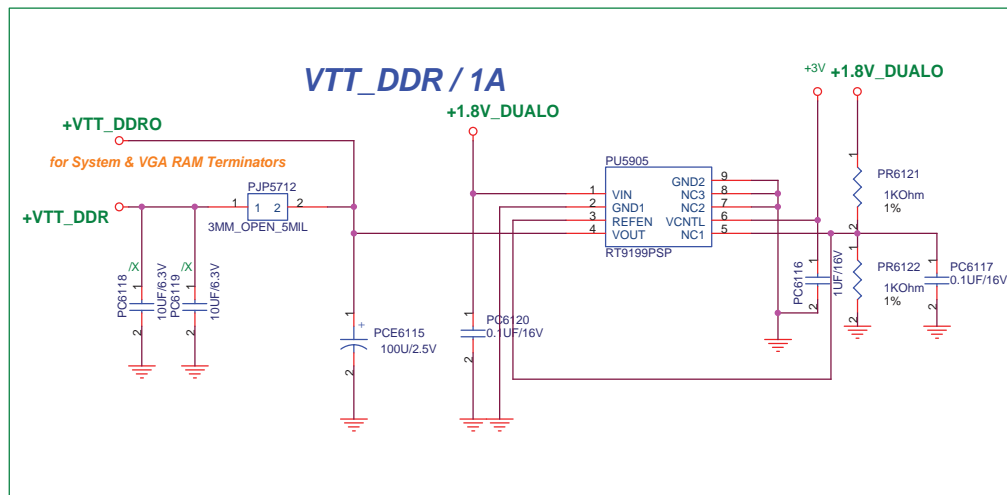


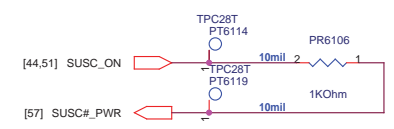
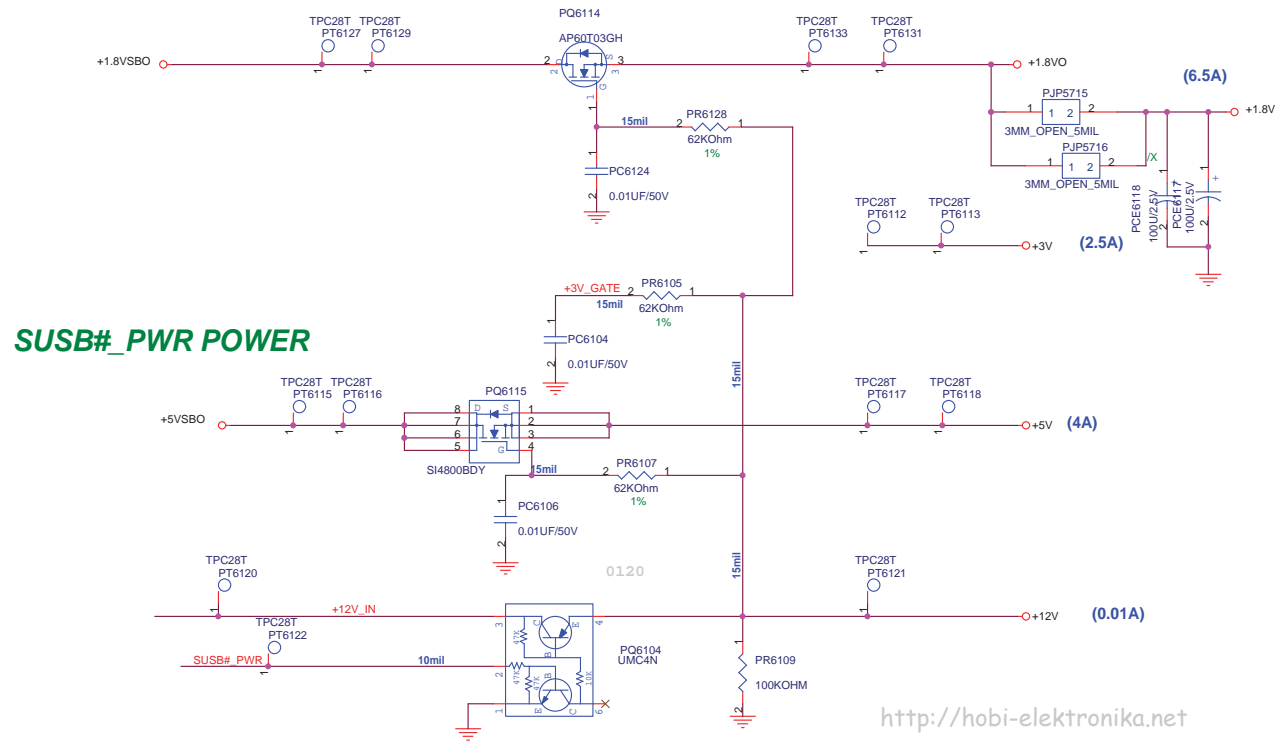
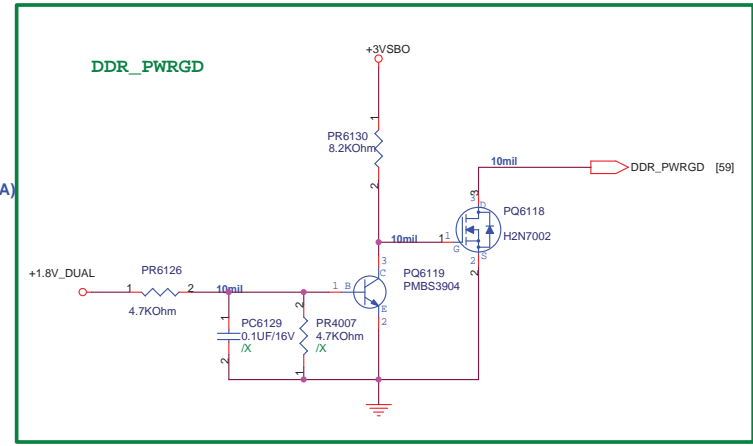
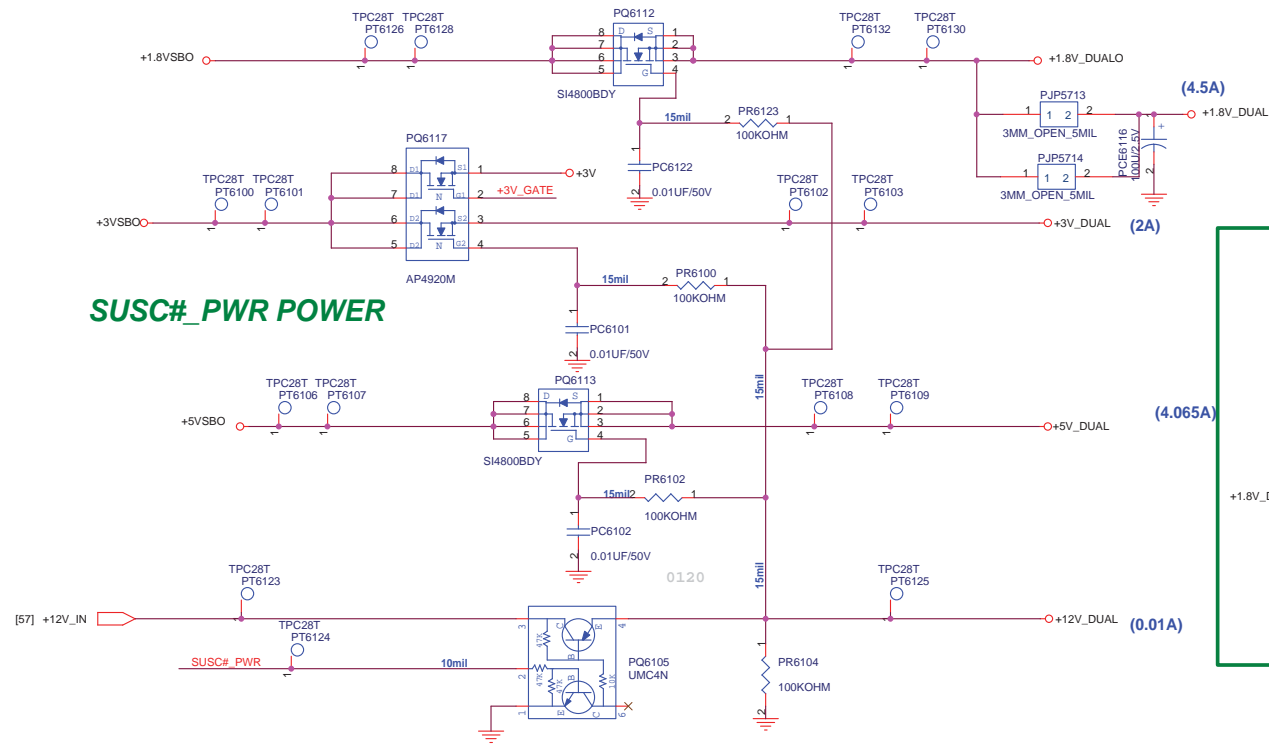
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